I³N Innovative Integrated Instrumentation for Nanoscience

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High Resolution Electronic Measurements in Nano-Bio Science

Measuring quantum devices below 4K

Cryogenic electronics

Giorgio Ferrari

Milano, June 2025

Outline

- Motivation for cryogenic electronics
  - Challenges
  - Design rules
- Examples

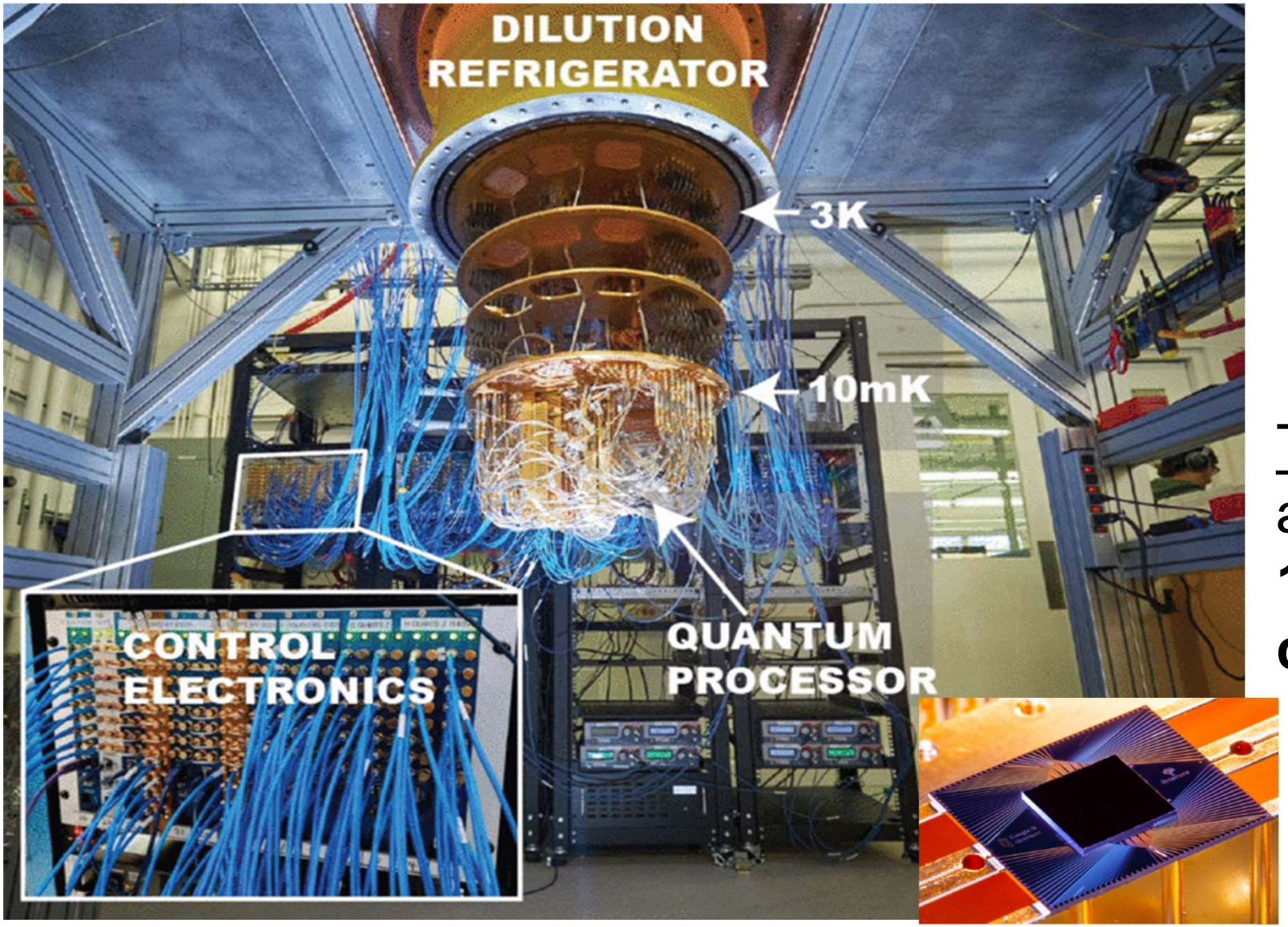
DiVincenzo criteria

Minimum requirements for the physical implementation of a quantum computer

- Robust, reproducible, and scalable qubit technology
- Qubit initialization
- Universal set of gates (single-qubit operations and two-qubit operations)
- Long-coherence time (figure of merit: number of gates before the state is lost for the environmental disruptions)
- Qubit measurement

[DiVincenzo 2000]

Google quantum computer (sycamore)



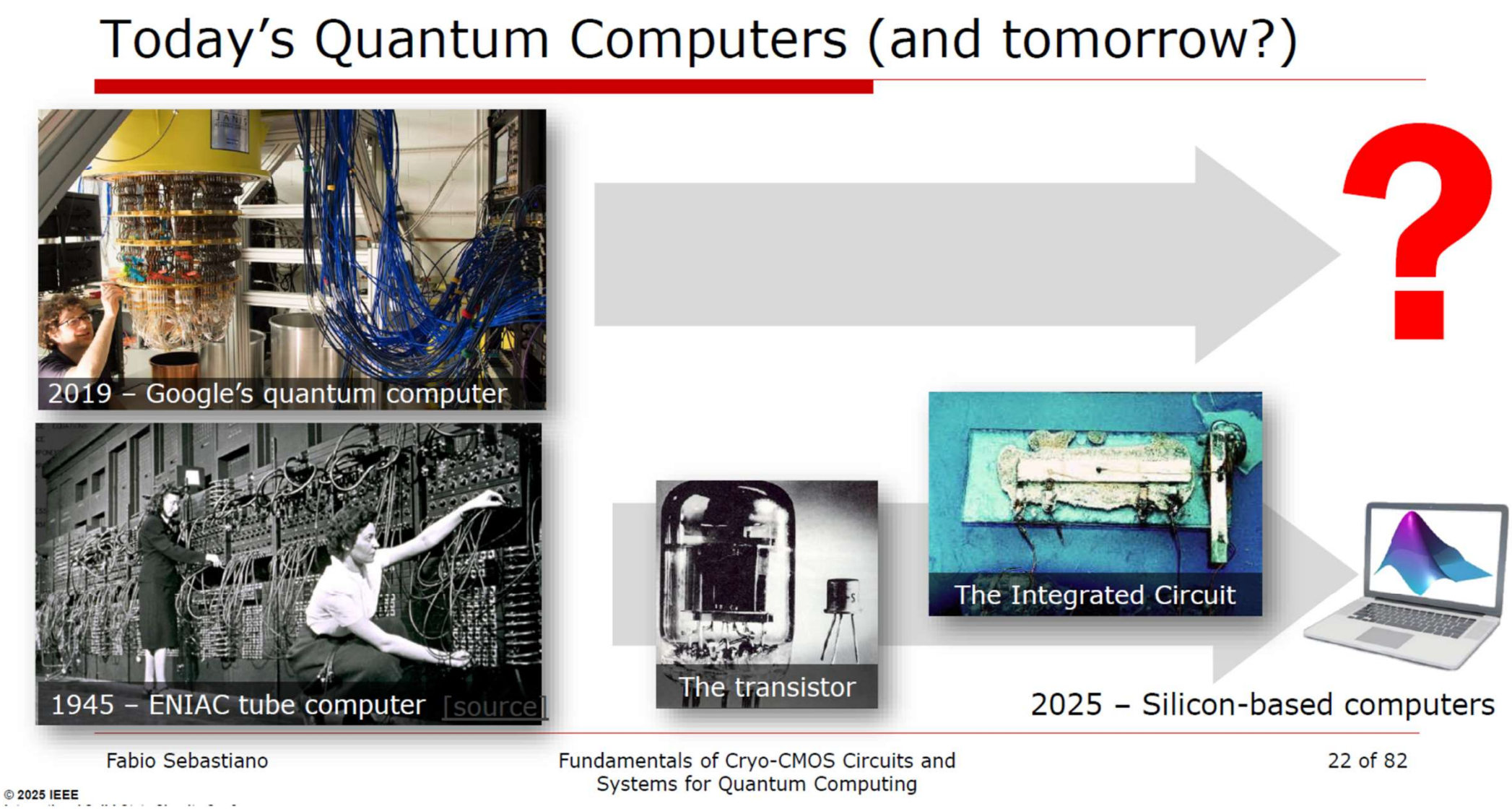
[J. Bardin, ISSSCC 2022]

54 qubits (transmons)

Target for useful applications: **10^6 physical qubit!!!**

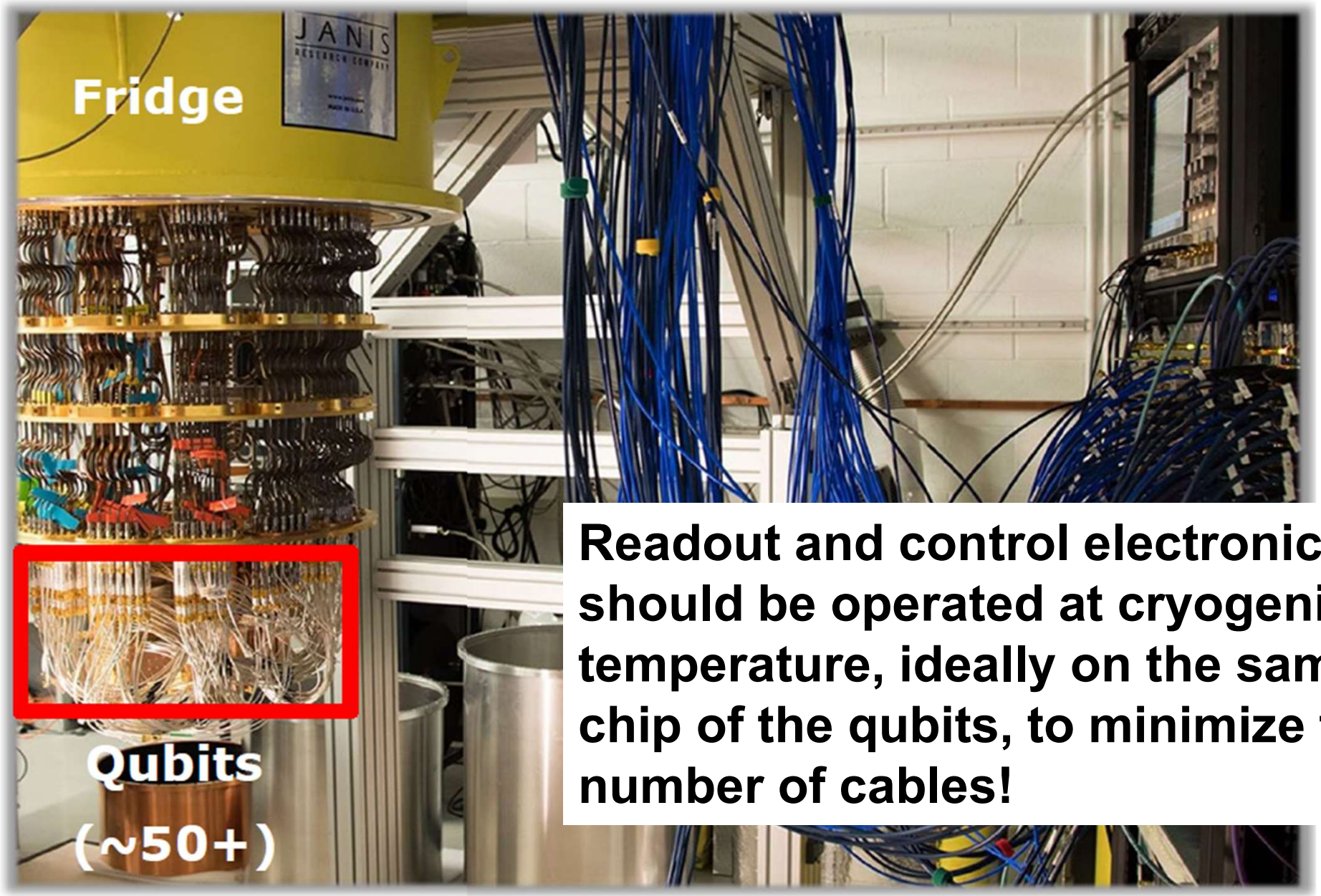
Cables connecting qubits (≪4K) to room temperature electronics are a limiting factor! (≈ 2 coaxial cables /qubit)

How to scale up QCs?



[F. Sebastiano, ISSCC 2025]

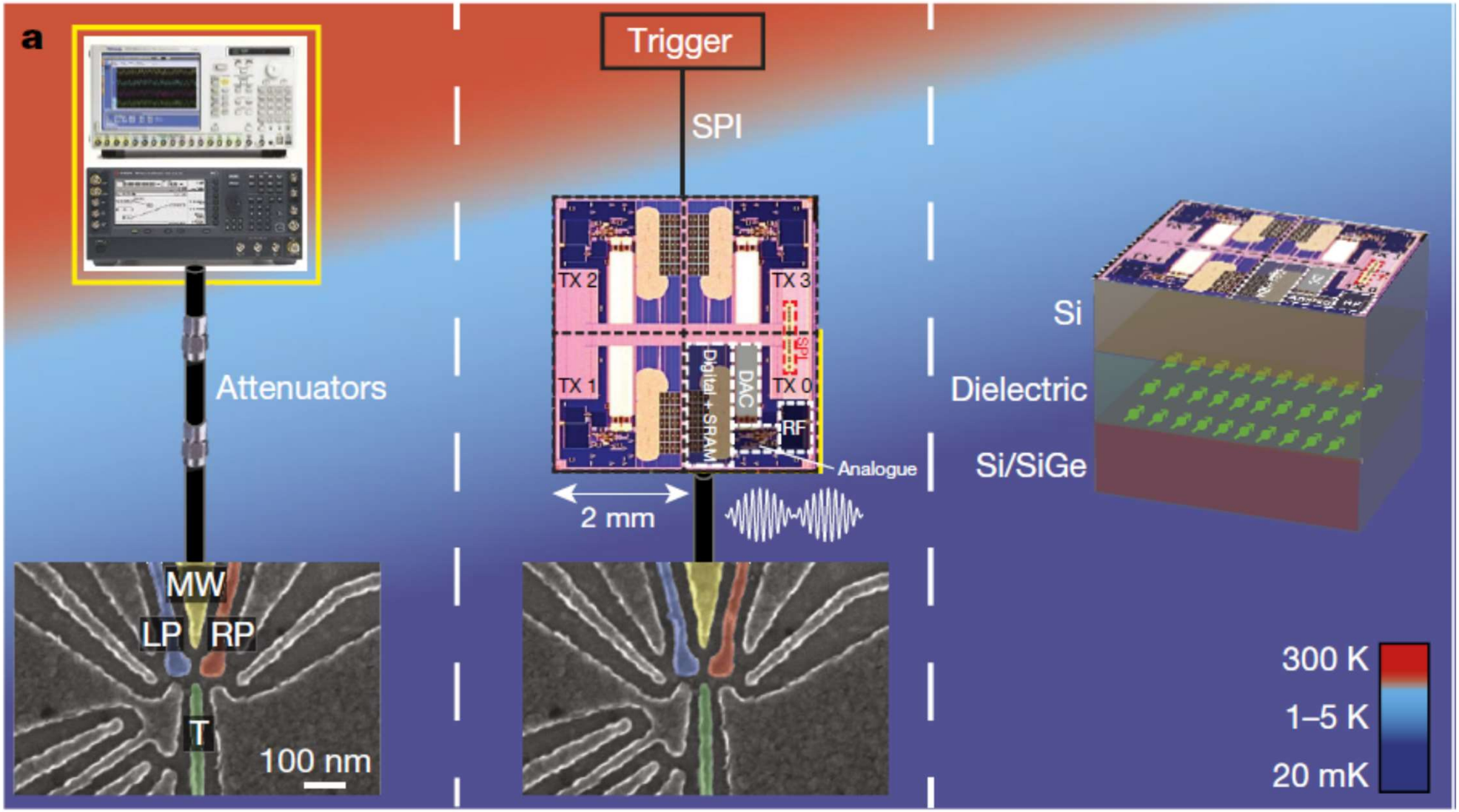
The role of cryogenic electronics



Readout and control electronics should be operated at cryogenic temperature, ideally on the same chip of the qubits, to minimize the number of cables!

[Bardin, ISSCC 2019]

Cryogenic quantum controller



Today Tomorrow Future

X. Xue *et al.*, "CMOS-based cryogenic control of silicon quantum circuits," *Nature*, pp. 205–210, 2021

Outline

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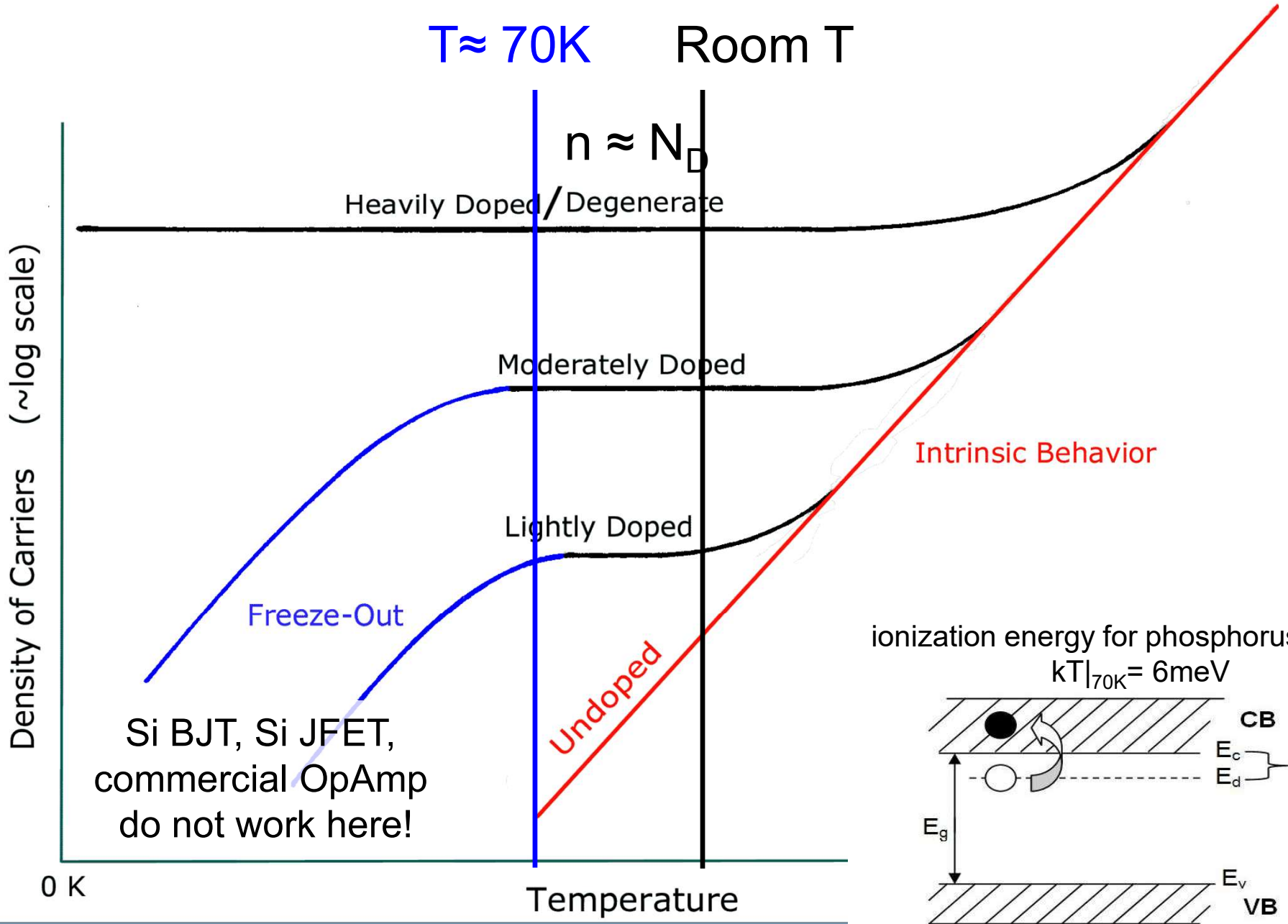
Freeze-out and degenerate semiconductor



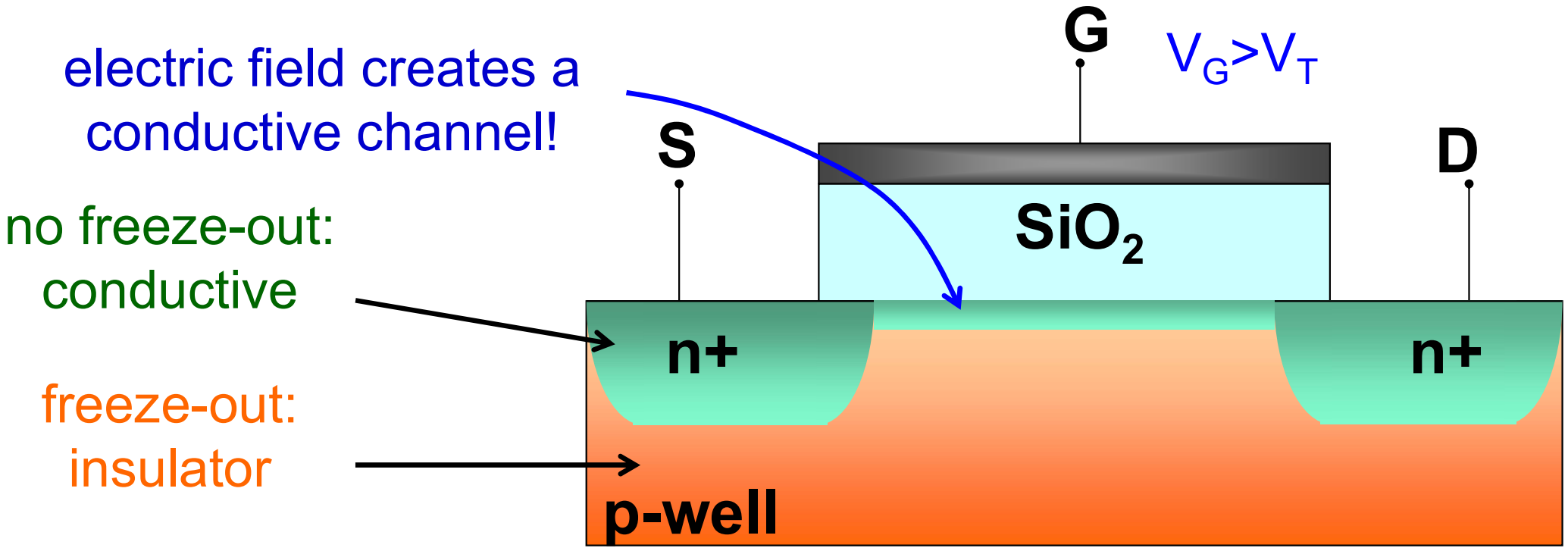
http://www.extremetemperatureelectronics.com

ionization energy for phosphorus: 45meV

$kT|_{70K}$= 6meV

http://fog.ccsf.cc.ca.us/~wkaufmyn/

Electronics below the freeze-out temp.

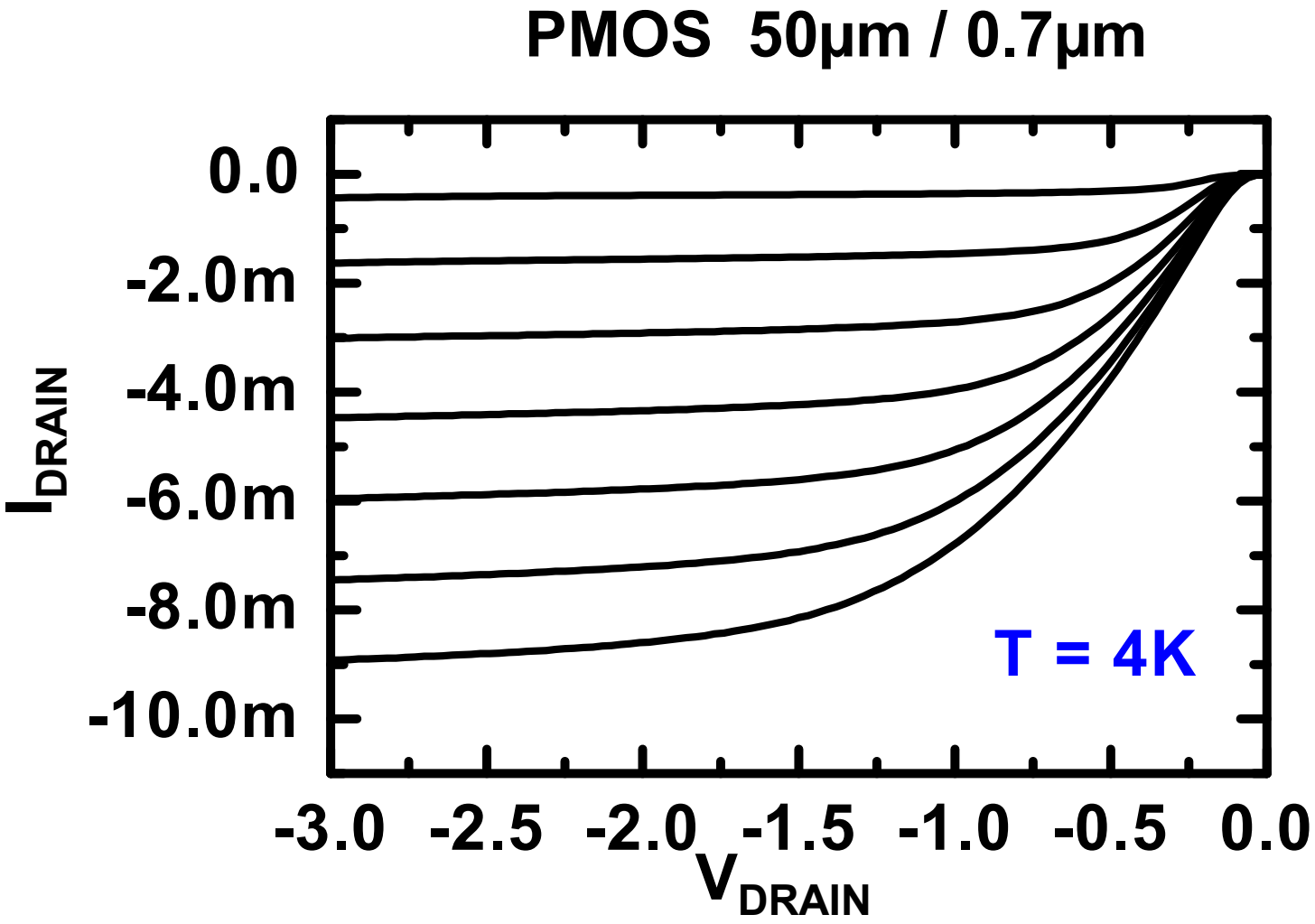


Silicon MOSFETs in standard tech. operate below 40K!

Many GaAs devices operate at cryogenic temperature:
degenerate at 10^{16} cm^{-3}
Limitation: small (and expensive) scale integration

MOSFET operating at 4K

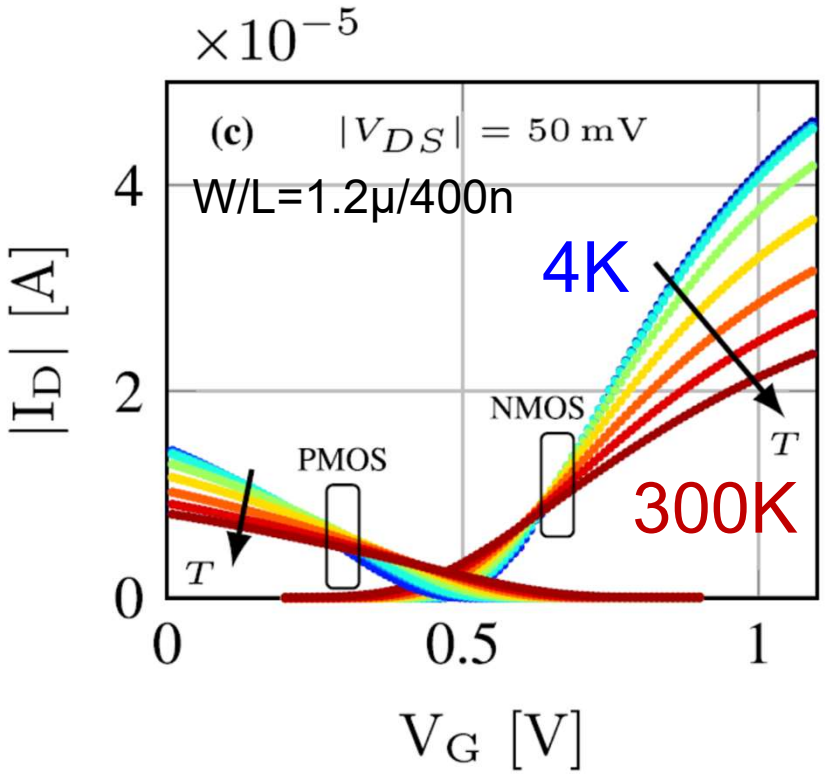
Standard analog CMOS Technology 3.3V, 0.35µm

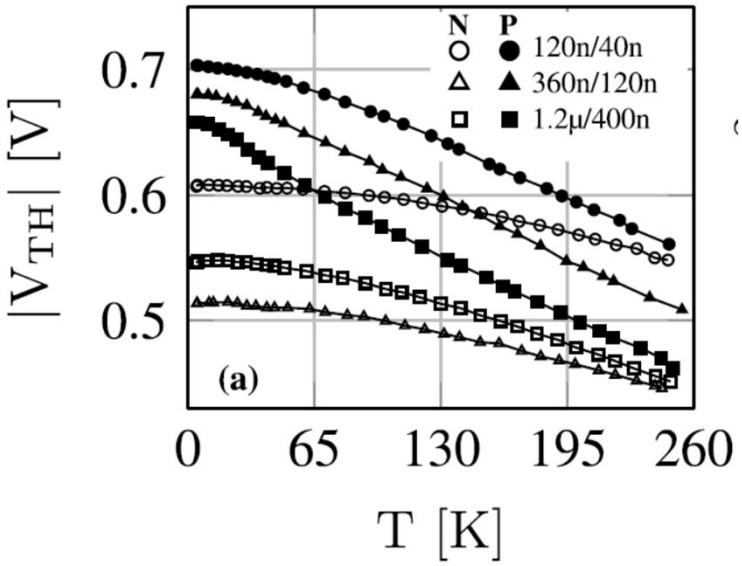


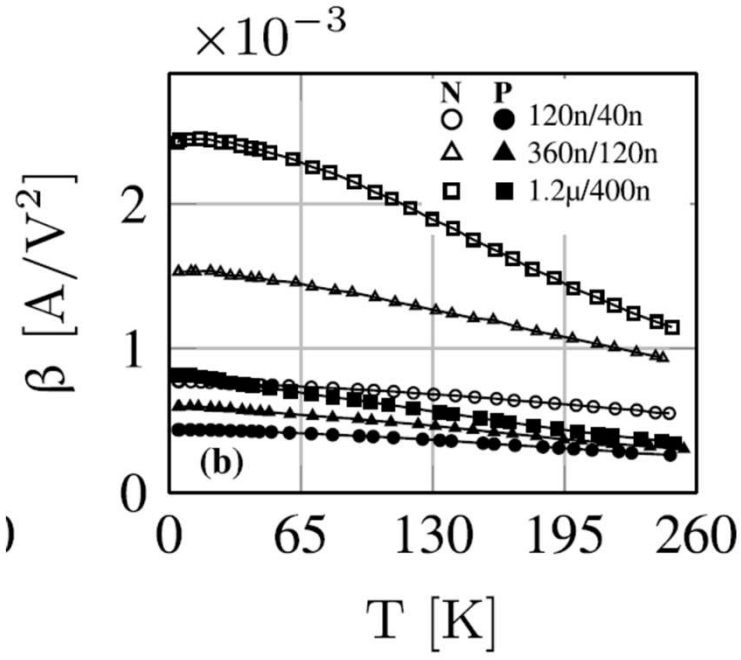
very similar to the room temperature behavior!

Effects of low temperature

TSMC 40-nm bulk CMOS process





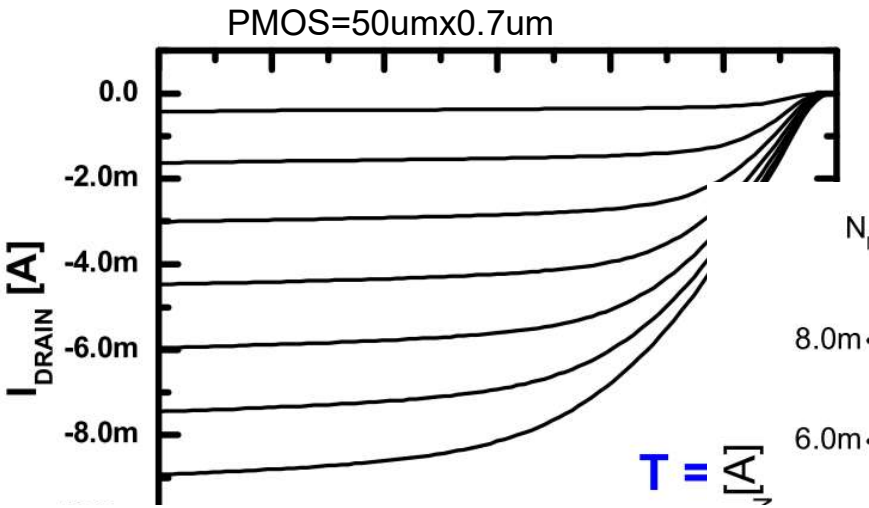


- substrate Fermi level shifts near to E_C (pMOS) → increase of the threshold voltage
- reduction in electron-phonon scattering → increase in carrier mobility

See also A. Beckers, et al. "Cryogenic MOS Transistor Model," *IEEE TED*, 2018.

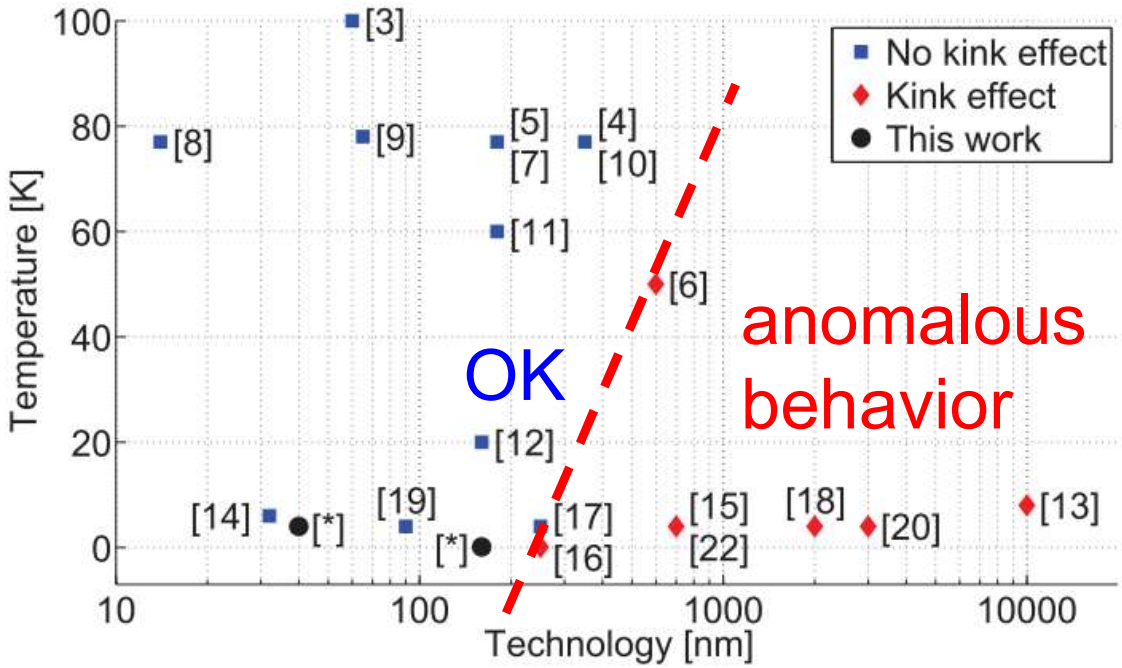
P. A. T'Hart, et al. *IEEE J. Electron Devices Soc.*, pp. 263–273, 2020]

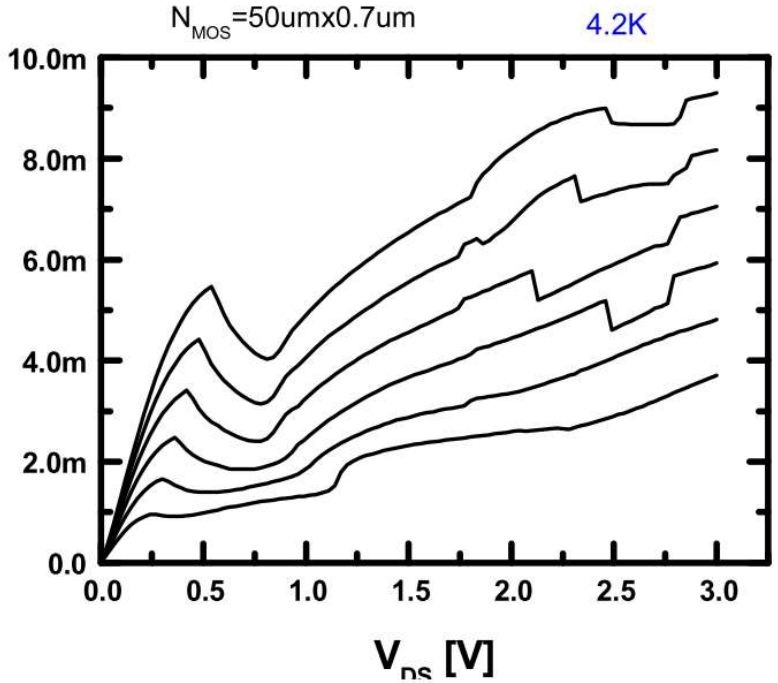
Problems are tech and size dependent



…and no models from the CMOS foundry!

AMS 0.35µm





Less problems using scaled technologies!

R. M. Incandela, et al.,pp. 58–61, 2017 ESSDERC.

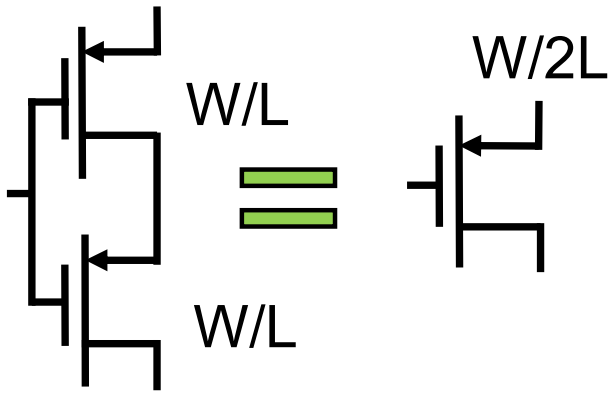
Design rule 1: characterize the technology!

No simulation models provided by the foundry

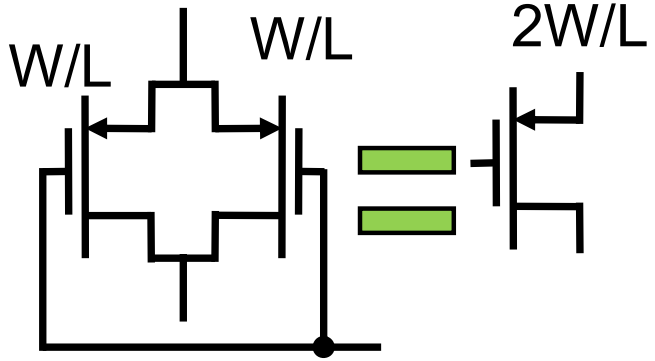
Experimental characterization of YOUR technology is MANDATORY

For simple circuits 1 nMOS and 1 pMOS is enough

series or parallel combinations of these basic transistors

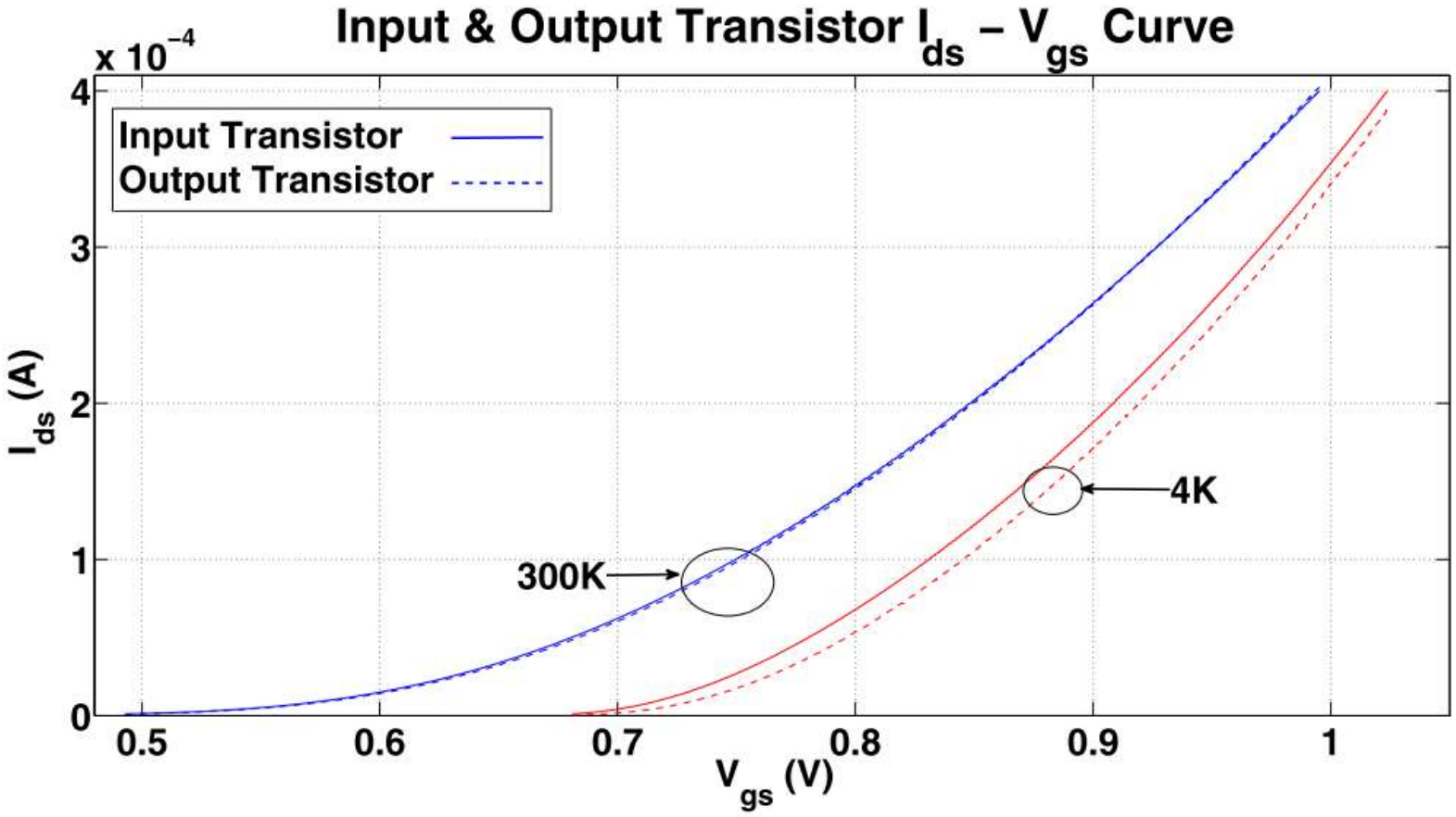


less conductive MOS



more conductive MOS

Design rule 2: pay attention to mismatch!

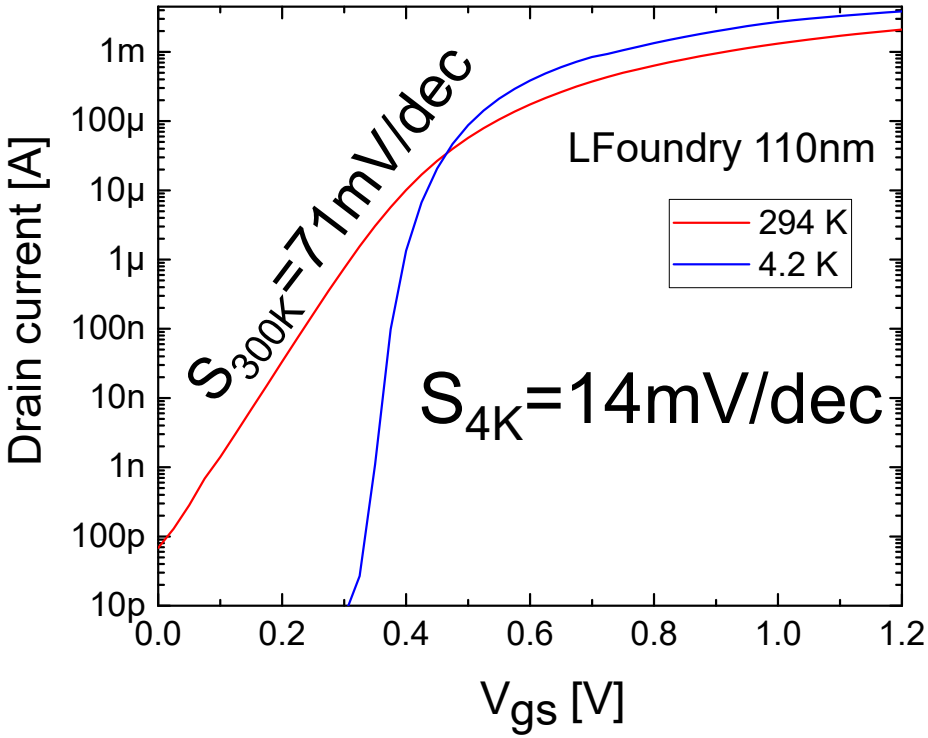


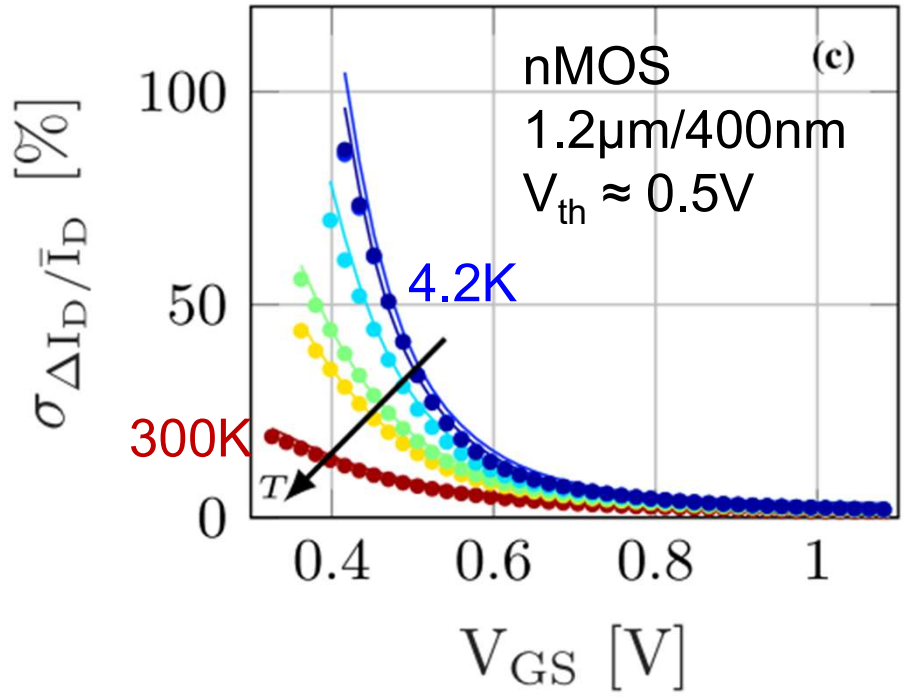
K. Das et al. EEE Symposium on Circuits and Systems, 2010

worsening of mismatch by a factor of 1.5-3 at low temperature compared to room temperature (tech dependent).

➡ Degradation of the offset voltage, linearity of ADC, DAC, bias setting,…

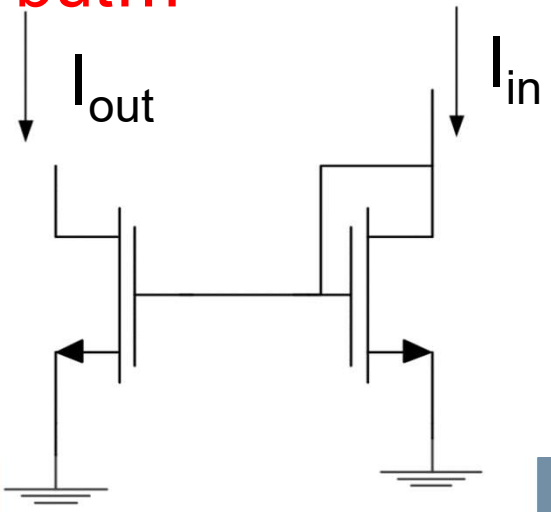
Design rule 3: subthreshold is critical





P. A. T'Hart, et al. *IEEE J. Electron Devices Soc.*, pp. 263–273, 2020

Higher g_m and I_{on}/I_{off}, good!
but…



V_T mismatch of 5mV:

$$I_{out,300K} \approx I_{in}\, 10^{\frac{5mV}{S_{300K}}} = I_{in} \cdot 1.17$$

$$I_{out,4K} \approx I_{in}\, 10^{\frac{5mV}{S_{4K}}} = I_{in} \cdot 2.28$$

Design rule 4: limited headroom

LFoundry 180nm: parameters from 300K to 4K

- $V_{T,n}$ from 0.3V to 0.5V
- $V_{T,p}$ from -0.65V to -1.1V
- Power supply: still 1.8V
- no subthreshold

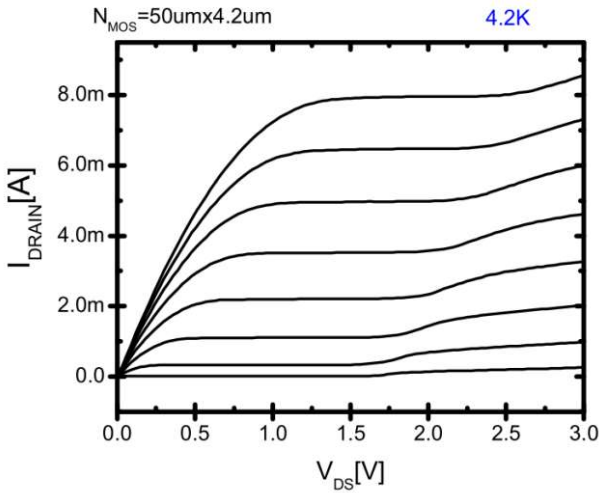
stack up few transistors!

and/or add complexity:

- Back-biasing if SOI tech. [Bohuslavskyi 2018]
- Feed-forward Body Biasing [Overwater 2023]

and

kink effect (old tech.)



limit the V_{DS}!

or use more scaled technologies

Noise

Thermal noise: $\overline{e_n^2} = 4kT\frac{\gamma}{g_m}$

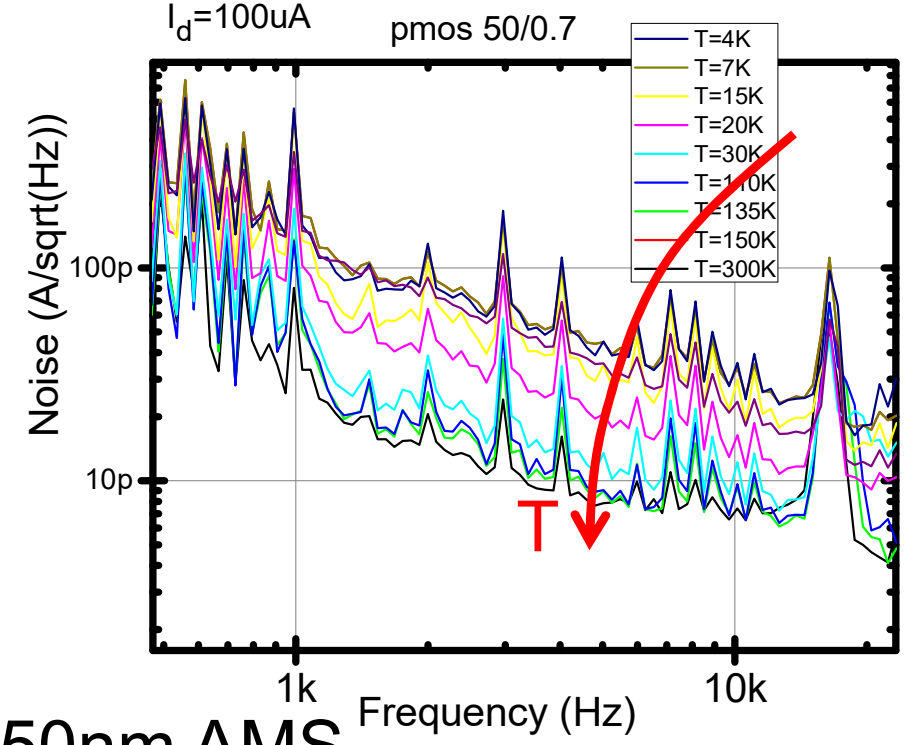
T ↘ , g_m ↗ → ***noise ↘ ↘***

(0.1nV/ √Hz)

For scaled tech.: white noise can be limited by **shot-noise** (T independent)
Self-heating: MOS channel can be at higher T (reported >40K for T_{amb}=4K)

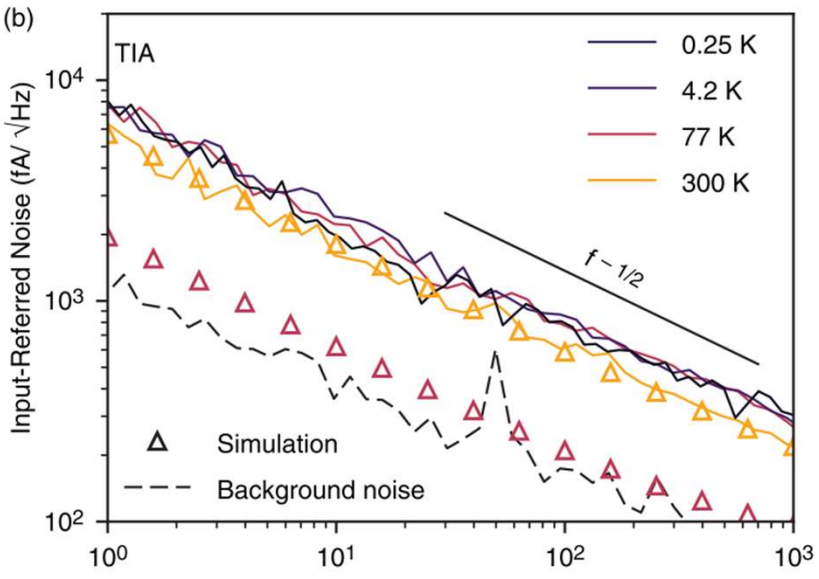
Flicker noise: increase or independent (tech and size dependent)

dominant noise up to tens of MHz



350nm AMS

28nm FDSOI tech.

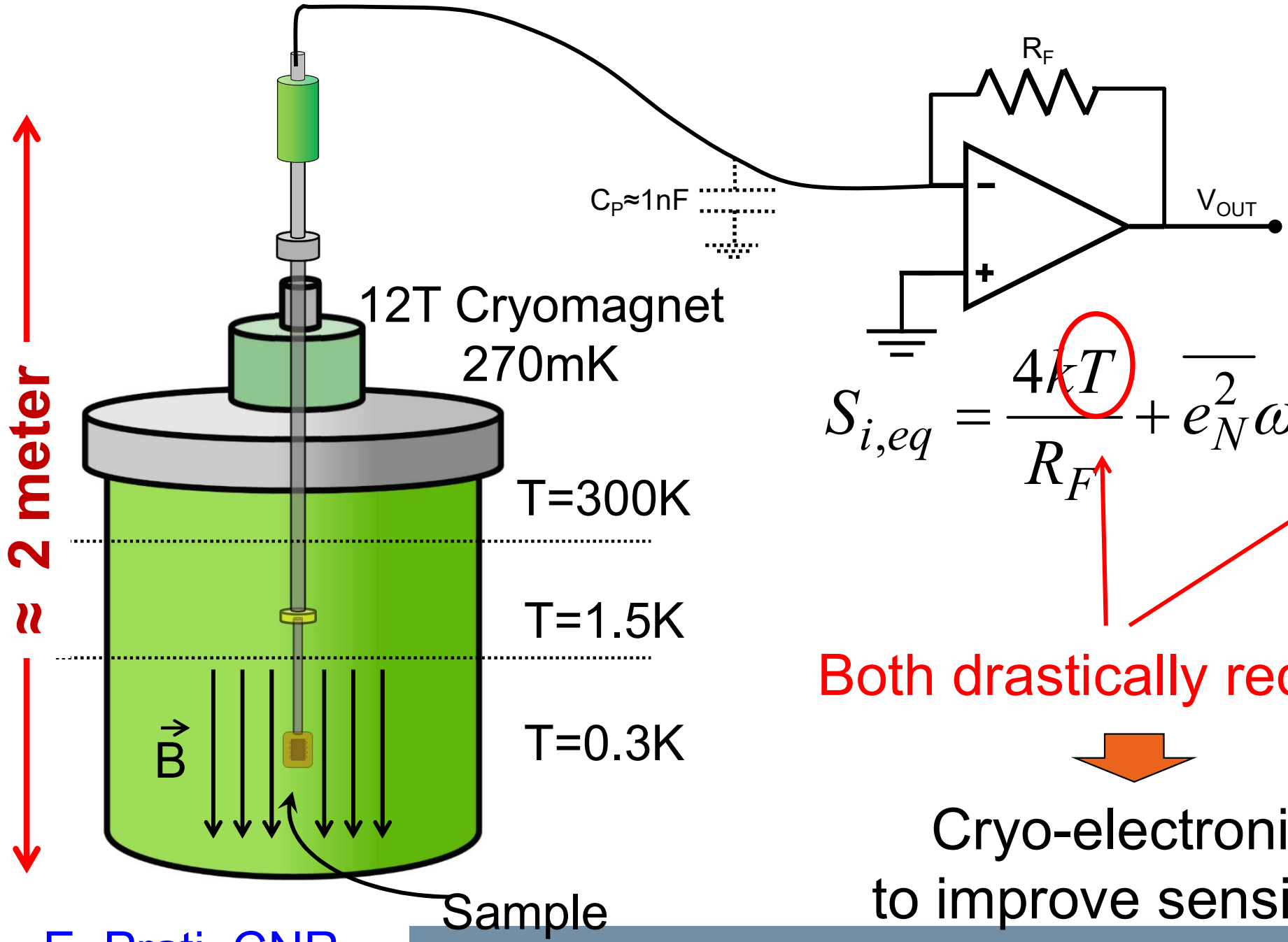


L. Le Guevel *et al.*, "Low-power transimpedance amplifier for cryogenic integration with quantum devices," *Appl. Phys. Rev.*, 2020

Outline

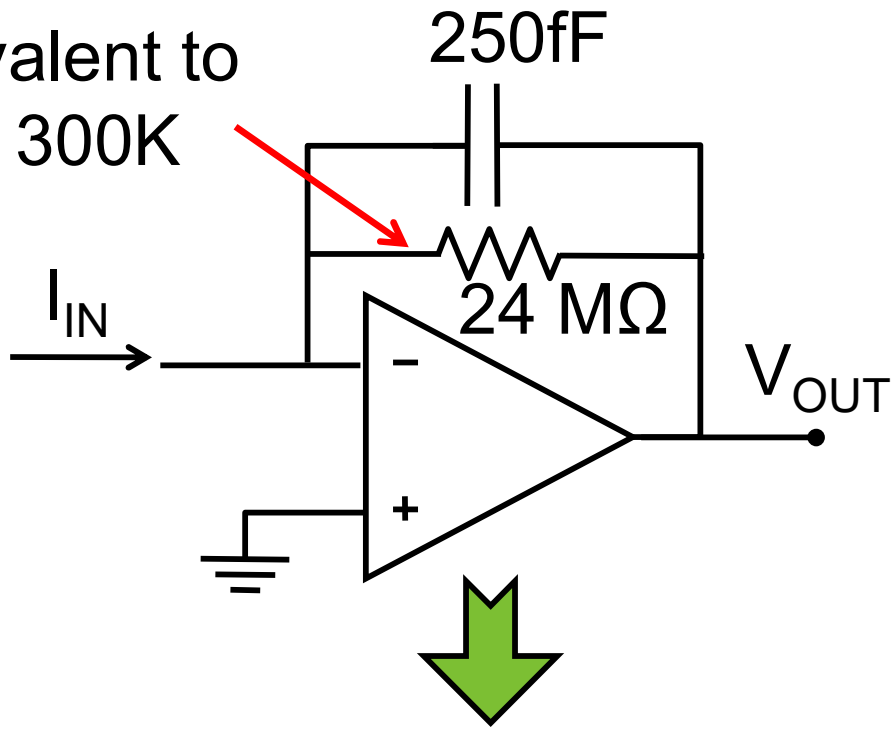
- Spin detection using room temperature instrumentation
- Cryogenic electronics
  - Challenges
  - Design rules
- Examples

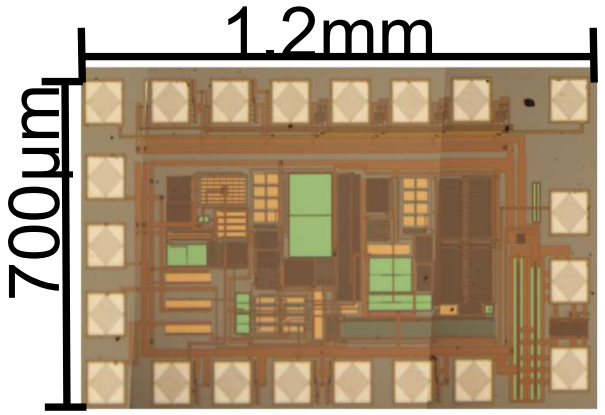
Experimental set-up to study quantum devices



Cryogenic transimpedance amplifier

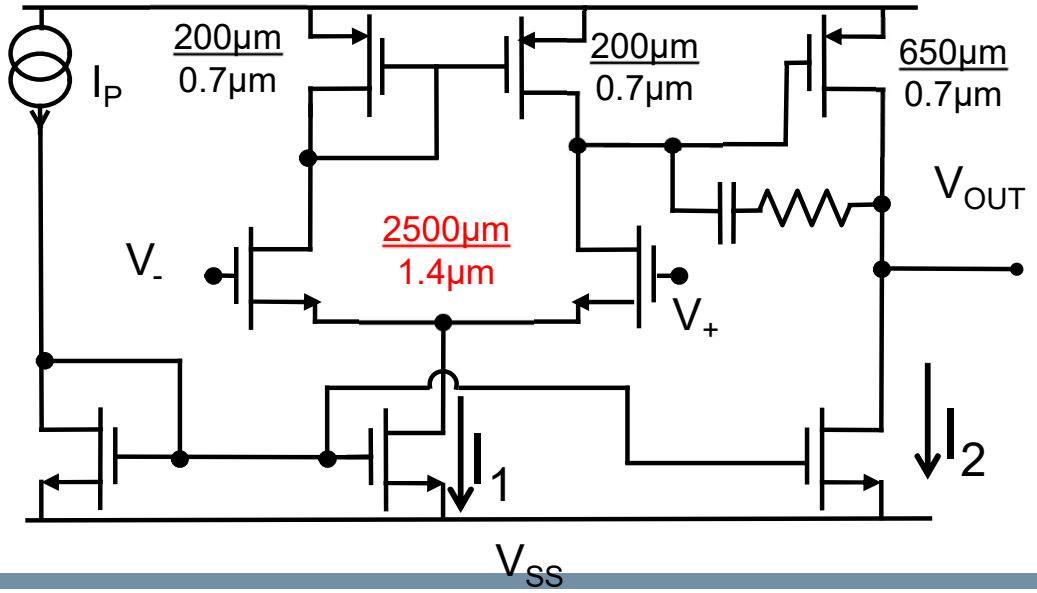
Noise equivalent to
1.7GΩ @ 300K





CMOS Technology
3.3V 0.35µm

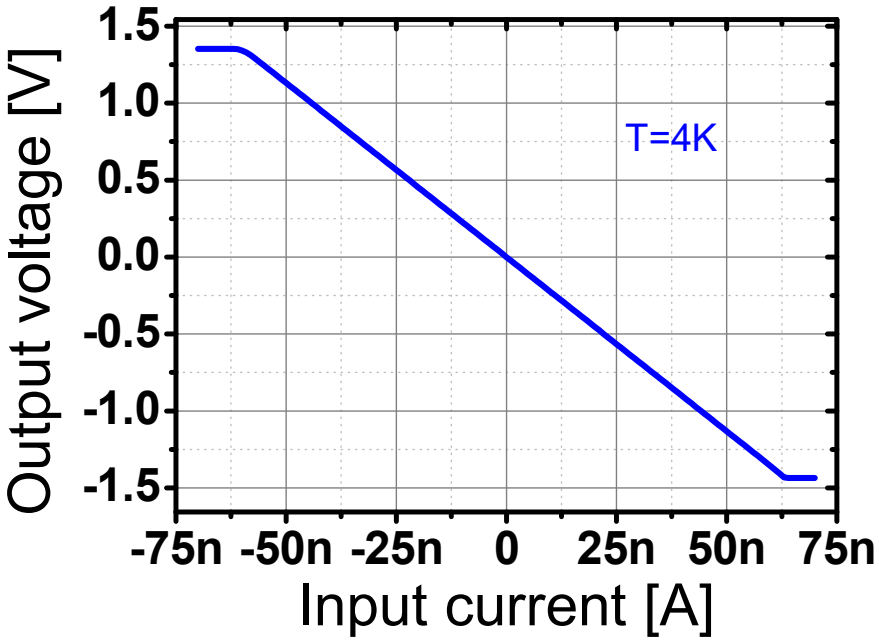
nMos: 50µm/1.4µm
pMos: 50µm/0.7µm



(simplified scheme)

F. Guagliardo et al., in "*Single Atom Nanoelectronics*", ed. E. Prati and T. Shinada, Pan Stanford Publishing (2013)

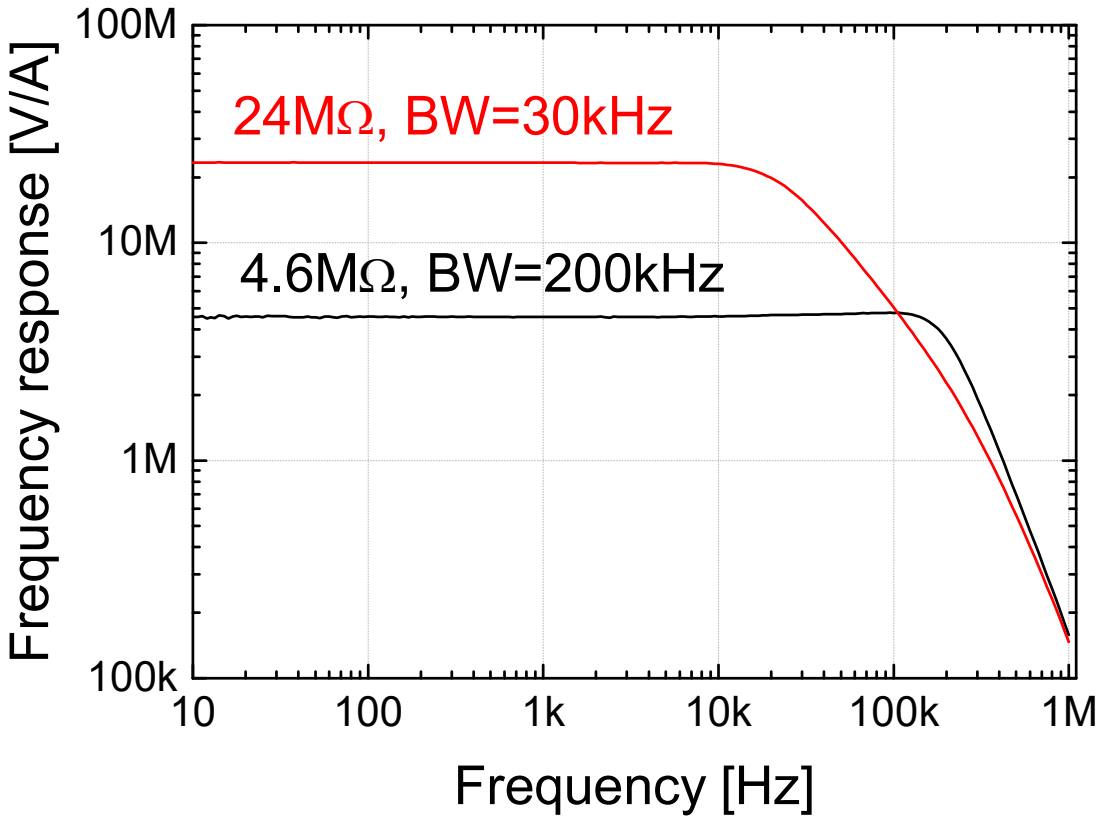
Measurements at 4 Kelvin



R still linear (10MΩ @300K → 24MΩ @ 4.2K)

C is practically unaffected by temperature

Gain, linearity and bandwidth match the simulations



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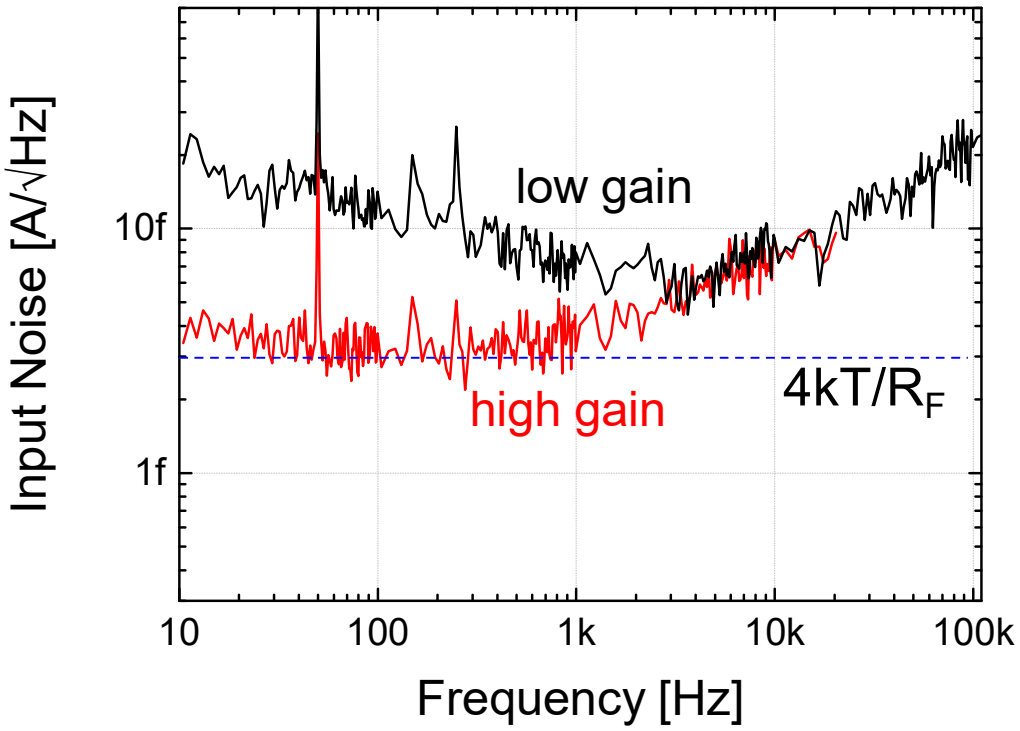
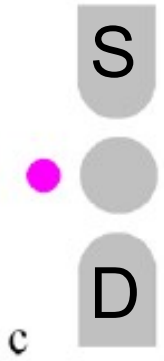
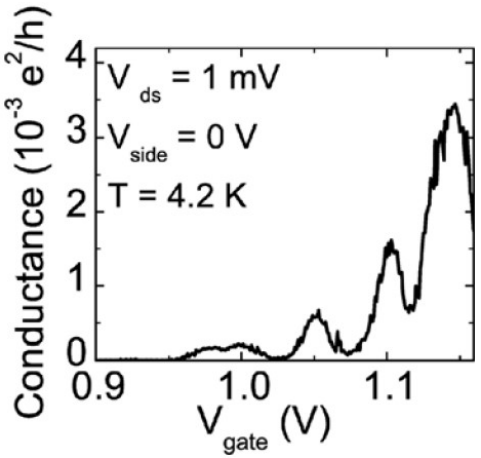


Quantum dots with a single ion implanted

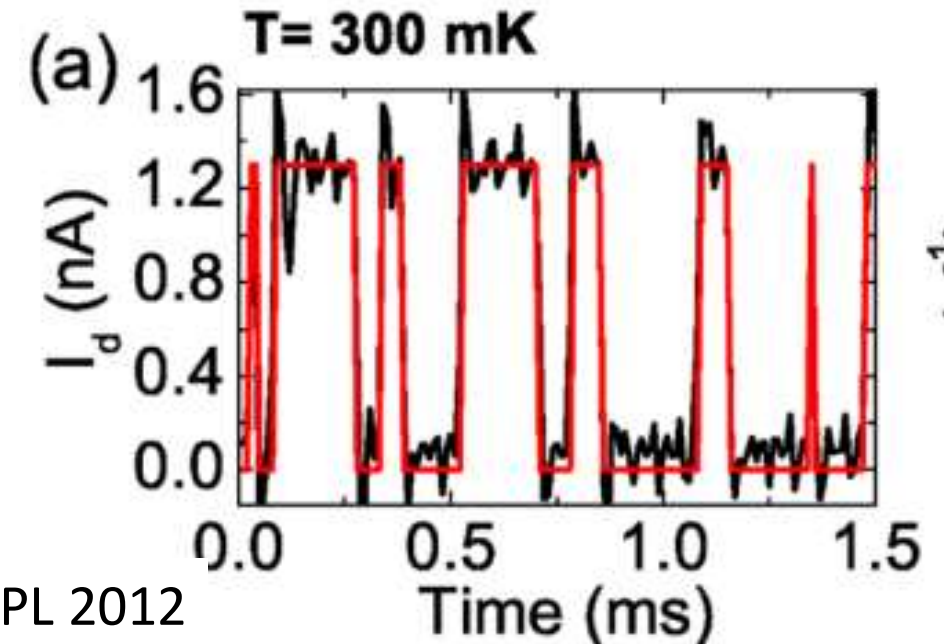




Single charge state sensing

- 2.3 pA_{RMS} resolution (14 pA)
- 32 kHz Bandwidth (190 kHz)

≈ 30 times better of RT

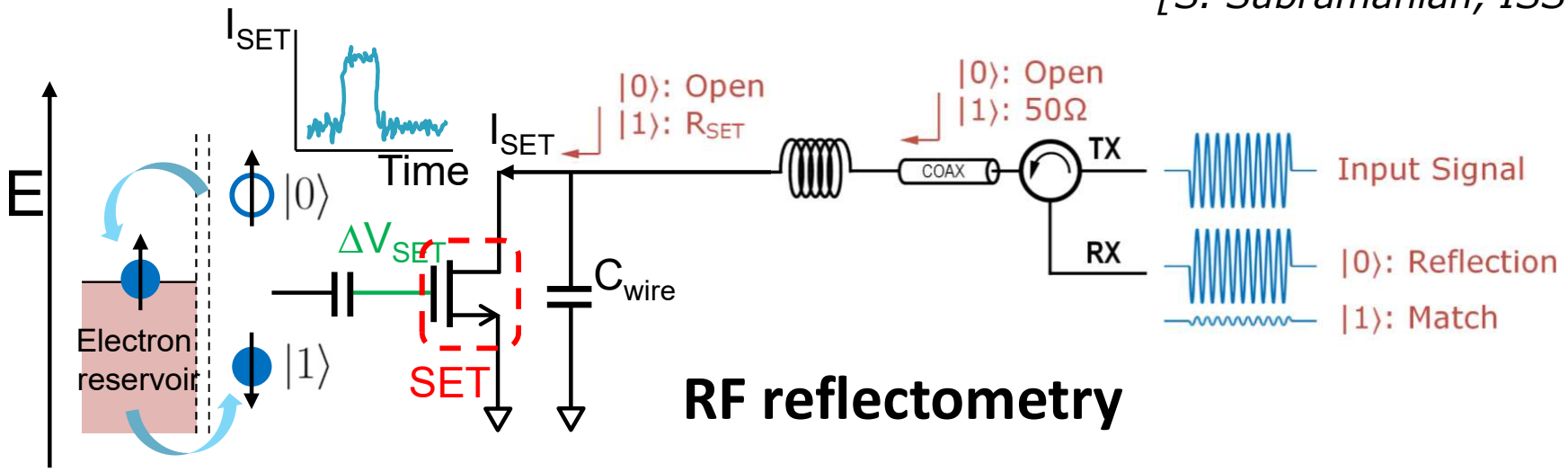


M. L. V. Tagliaferri et al, *IEEE Trans. Instrum. Meas.*, pp. 1827–1835, Aug. 2016.

Mazzeo et al APL 2012

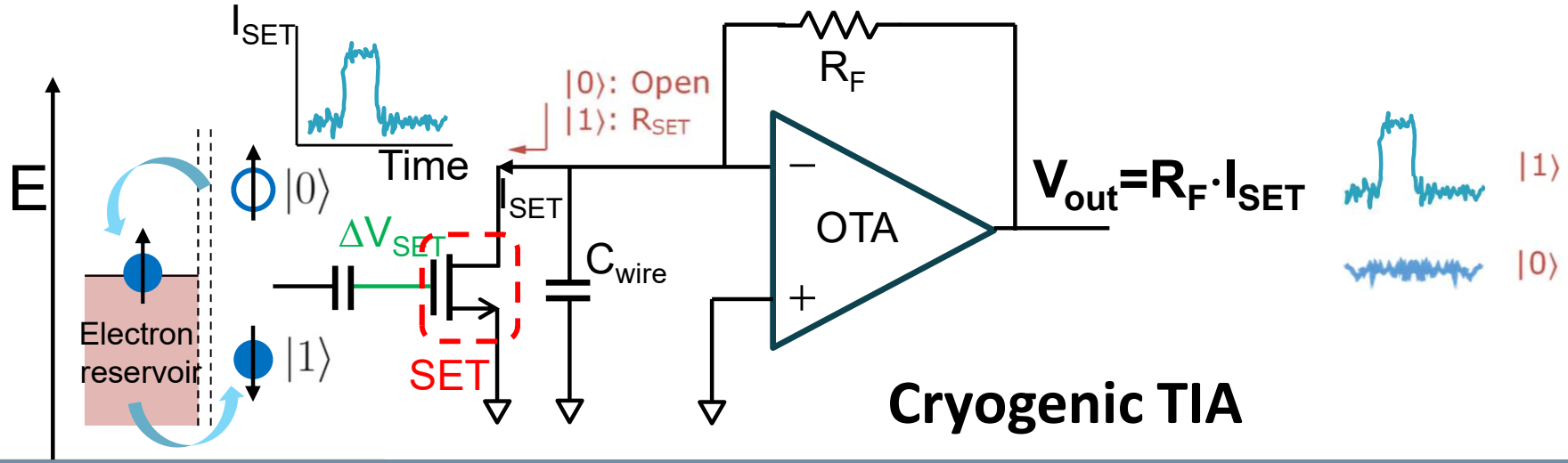
Spin qubit readout: measurement technique

[S. Subramanian, ISSCC 2023]



Bulky off-chip components, fast analog-to-digital converter, μ-wave signals

Fully CMOS-compatible readout operated at T<5K:



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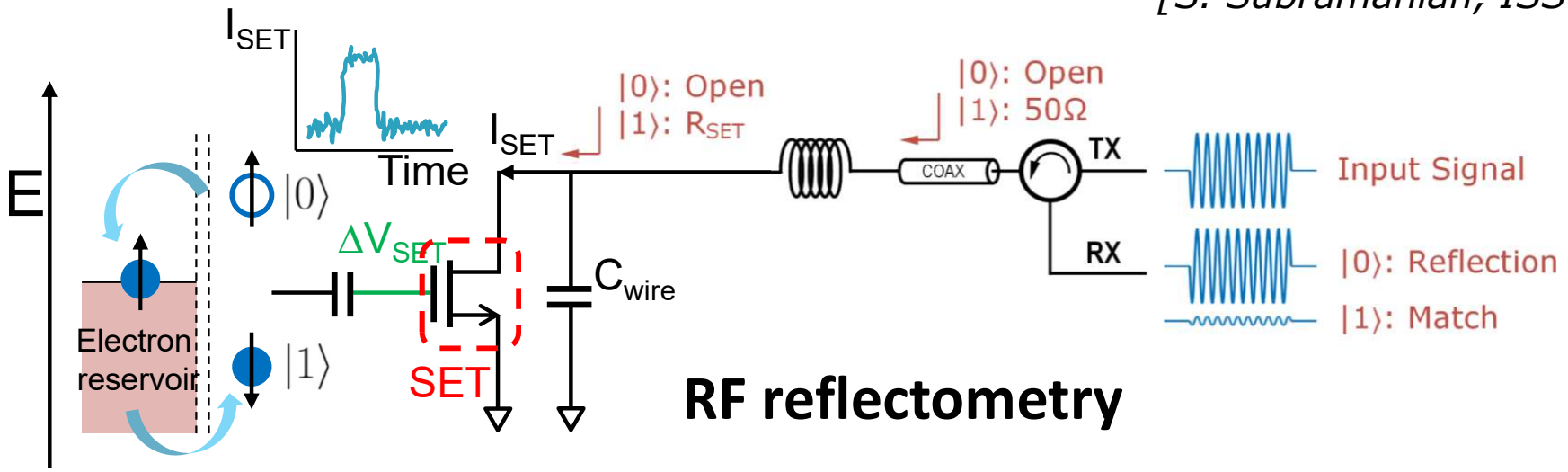

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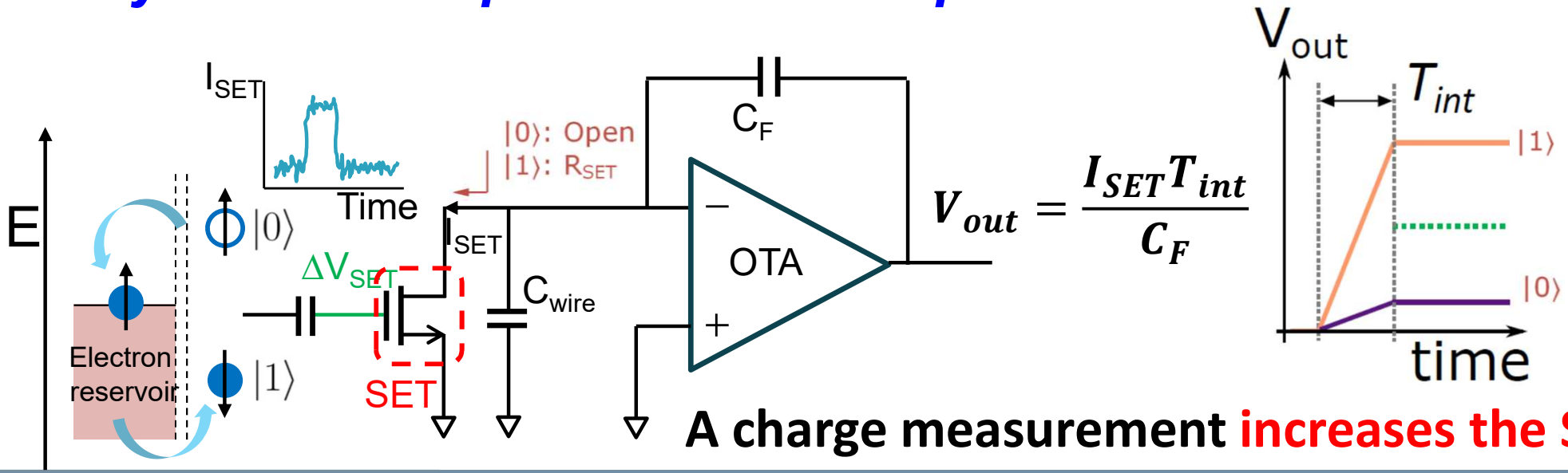
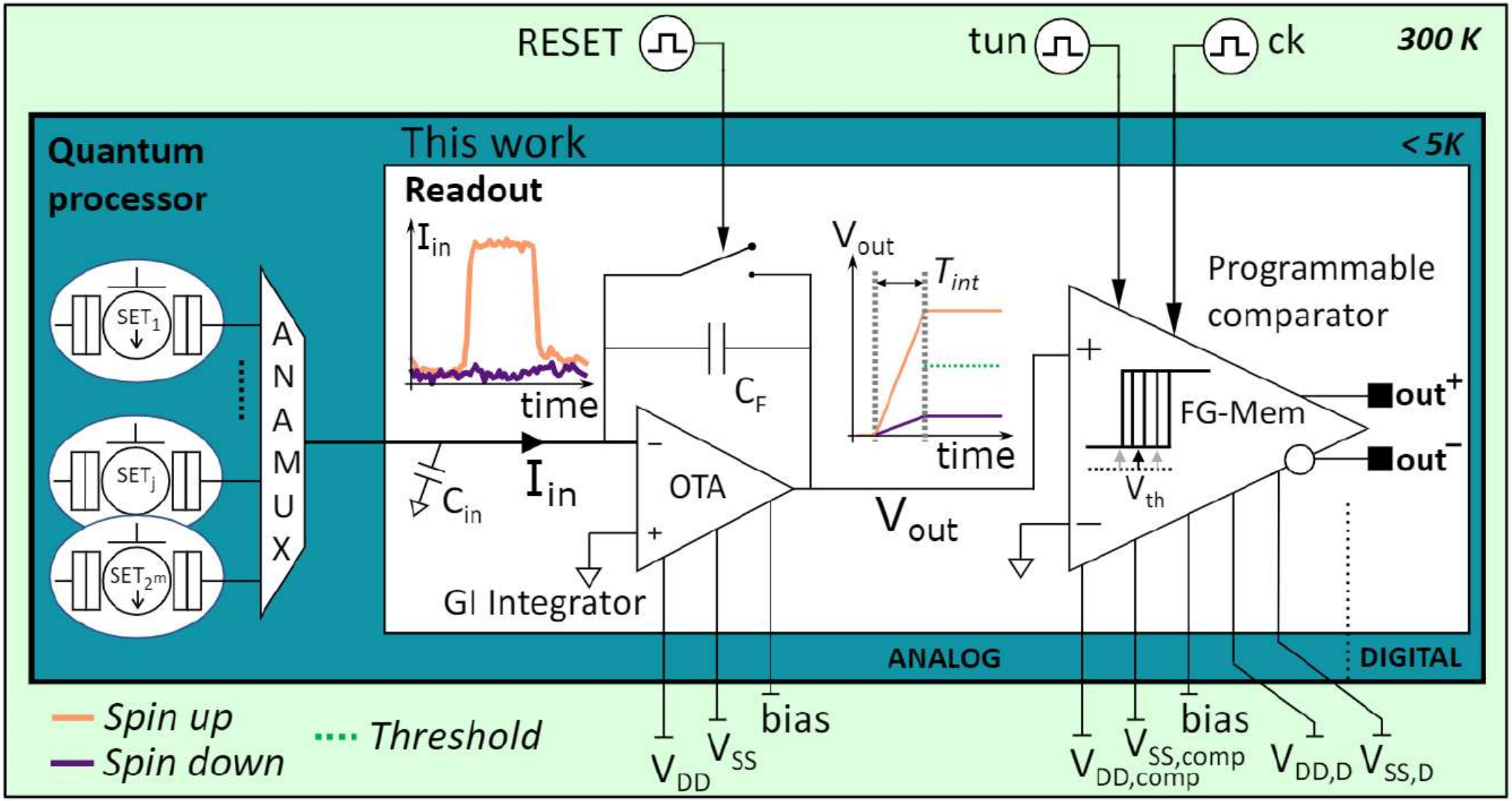


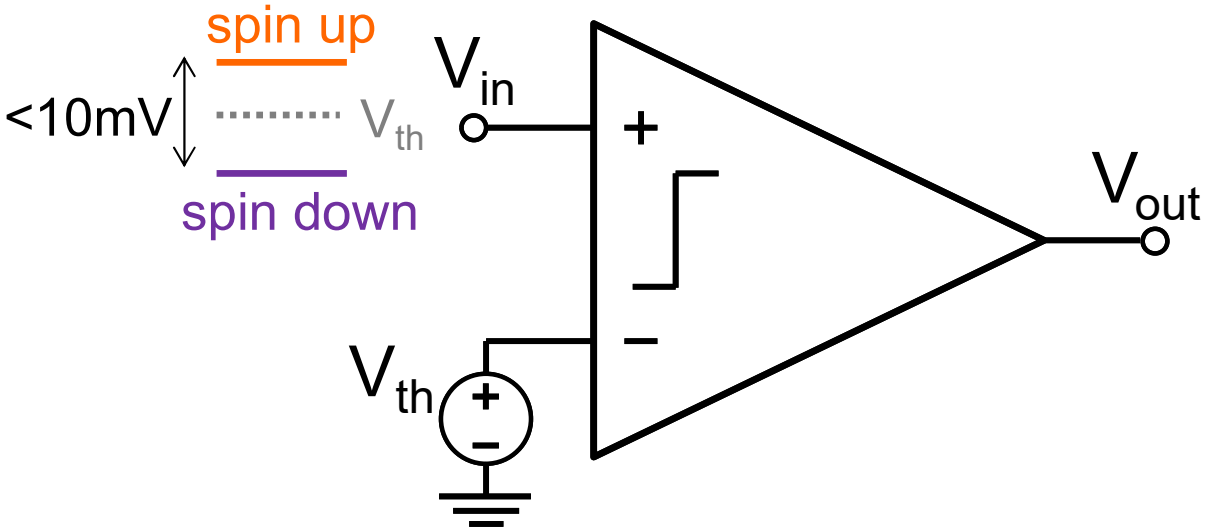
Compact readout based on current measurement

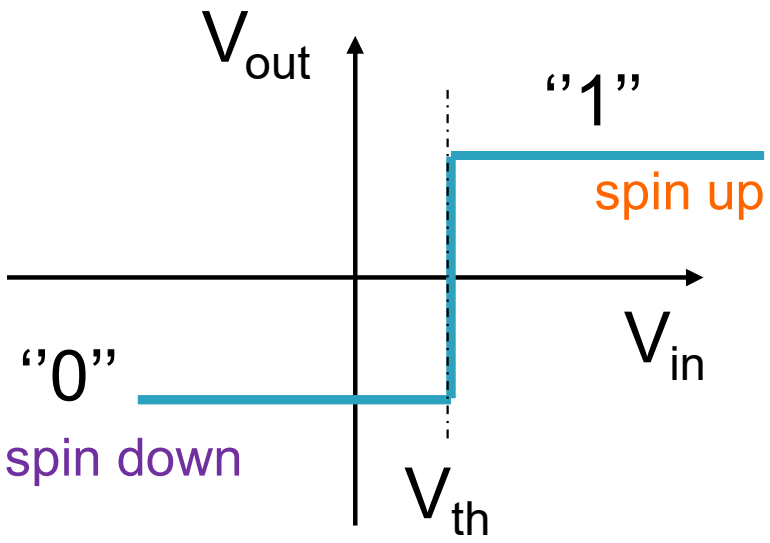


- Fully-integrated 150-nm CMOS technology (NO inductor or μw comp.)
- Direct charge-to-digital conversion
- Time division multiplexing architecture
- Low power consumption (1 mW/qubit)

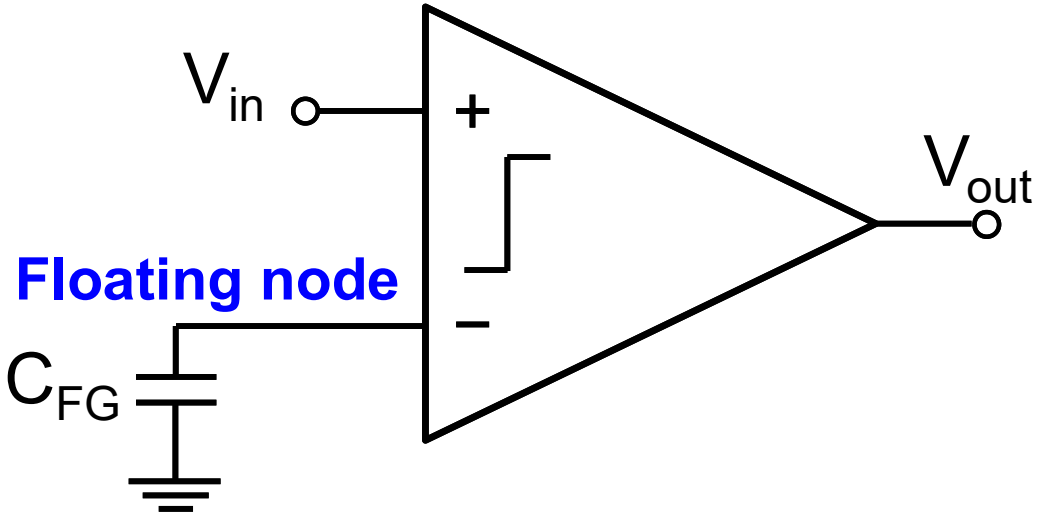
[M. CASTRIOTTA et al., IEEE *Solid-state Circuits Letters* (2023)]

Programmable floating-gate comparator





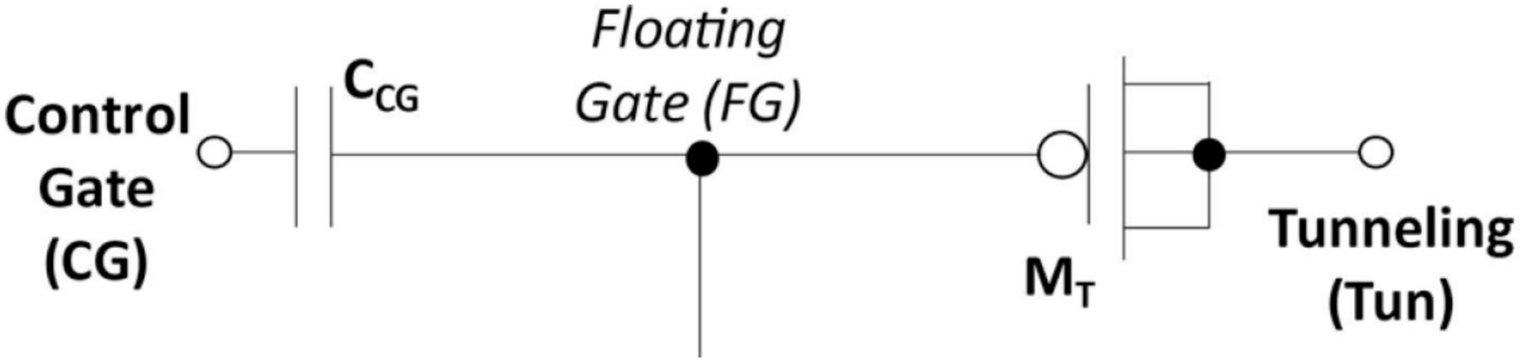
- V_{th} few mV! Process variations are critical
- Digital-to-Analog Converter (DAC): power consumption, size

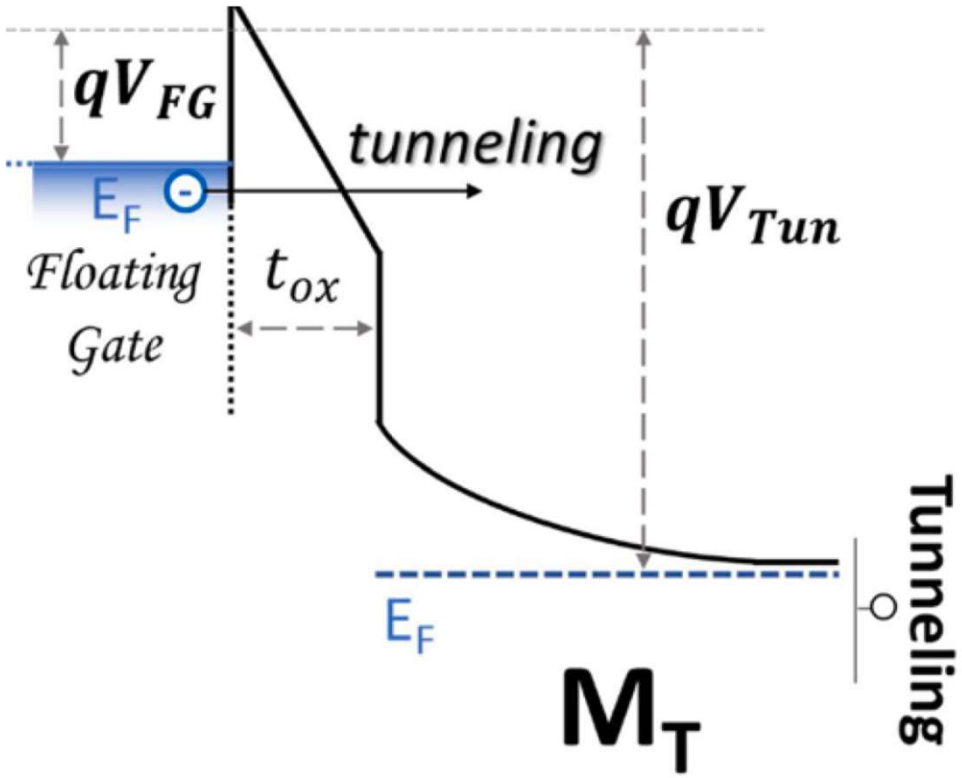


- Floating node charged at V_{th}
- Compact and low power

- How do we change the charge?
- How to compensate for the process variations?

Floating gate in standard CMOS technology

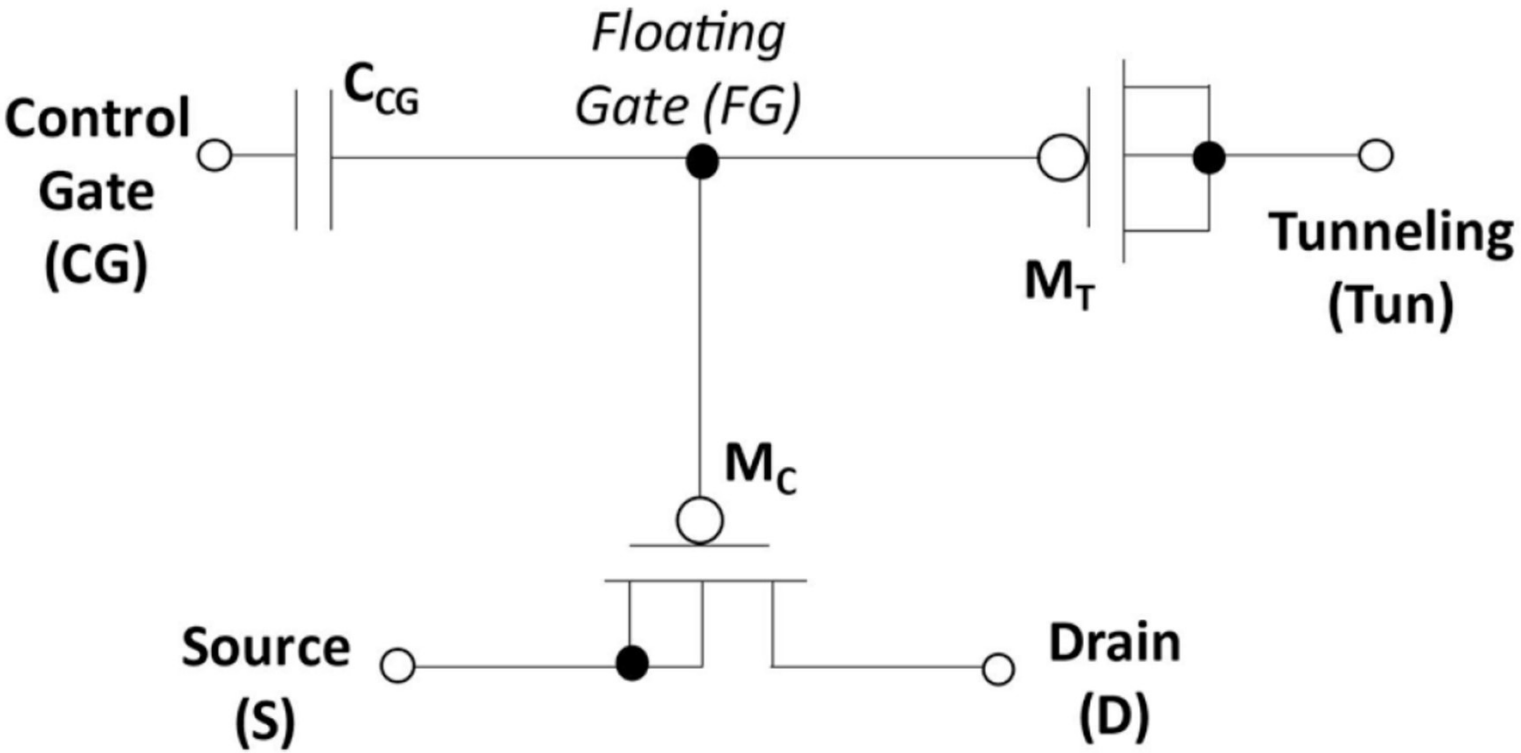




- It requires high voltages to enable tunneling (≈7V in our technology)

[M. Castriotta, Solid State Electronics 189 (2022)]

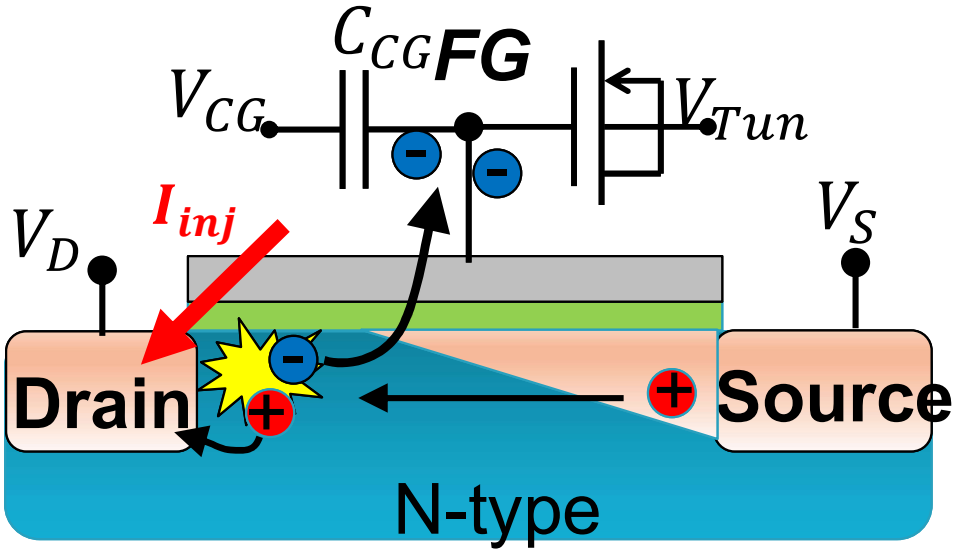
Floating gate in standard CMOS technology



- Hot electron injection using a p-type MOSFET
- The electrons are removed by tunneling (coarse global resetting of the floating gates)

[M. Castriotta, Solid State Electronics 189 (2022)]

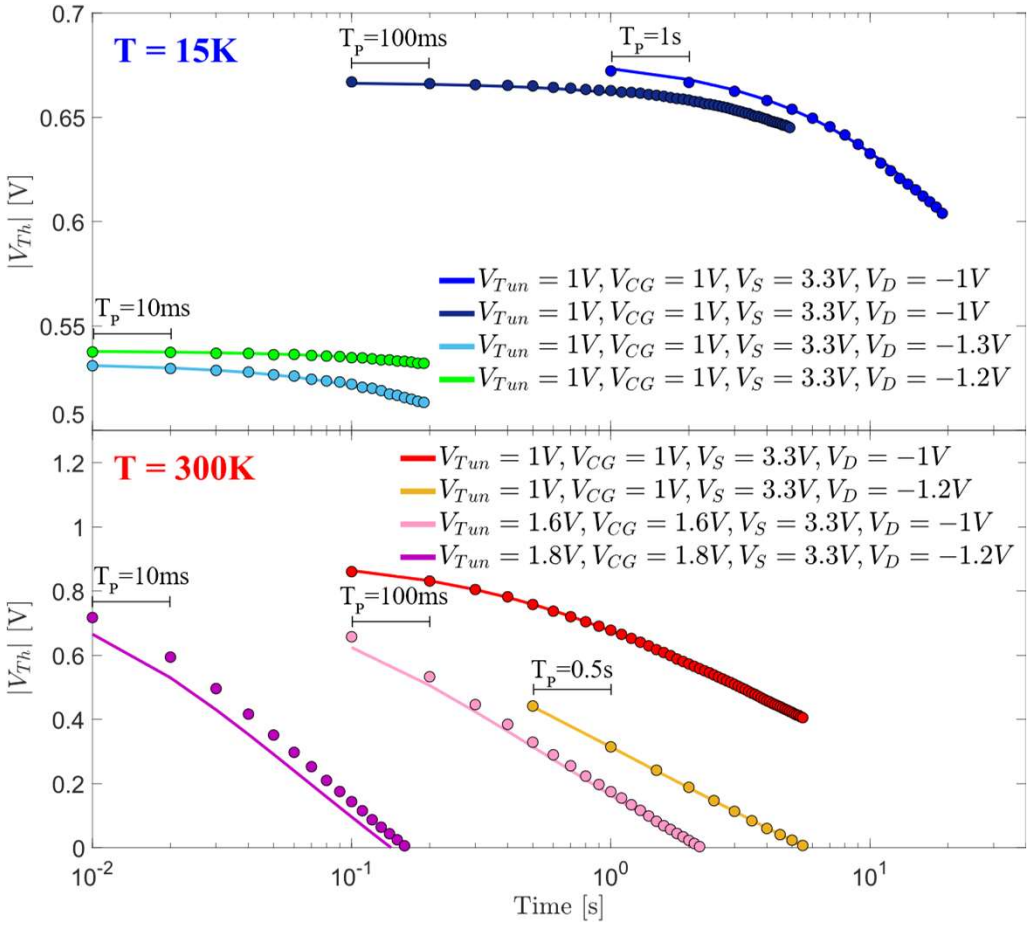
Hot electron injection in p-type FG transistor



holes collide with sufficient energy (≈ 3/2 E_{gap}) to liberate additional electron-hole pairs

- $V_{SFG}>|V_T|$ (ON)
- $V_{SD}>>0V$ (high electric field)
- $V_{SD}>>V_{SFG}$ ($V_{FG}>V_D$)

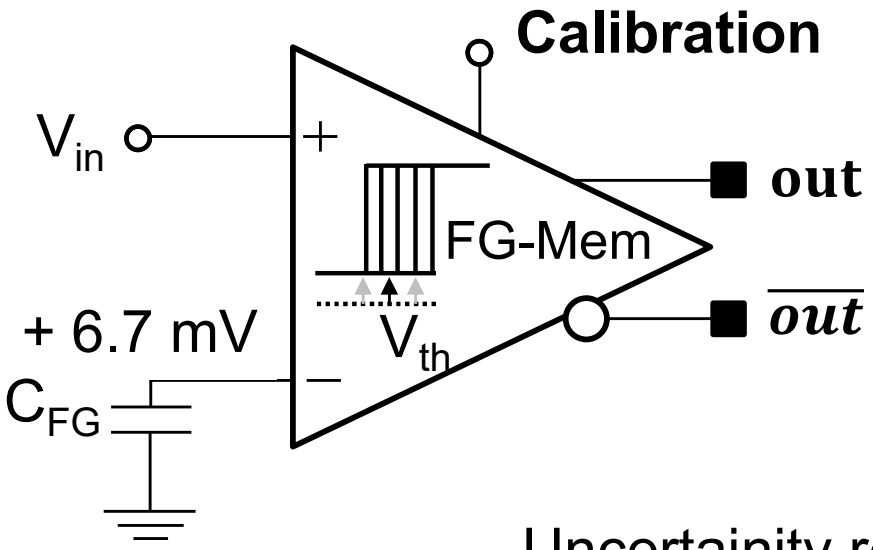
fine-tuning of floating node charge (i.e. threshold voltage of the FET)



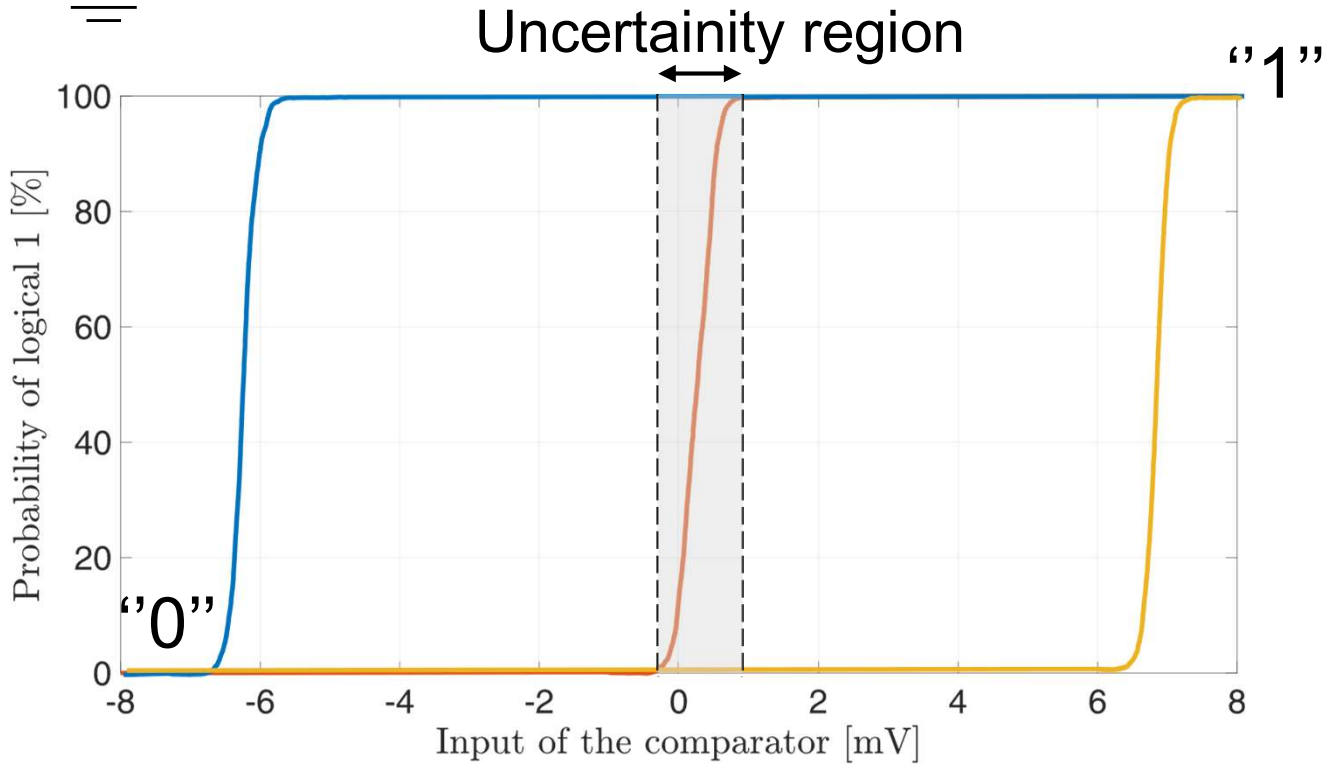
$$I_{inj} = C(V_{SD} - \gamma V_{ov})^3 I_d e^{-\frac{B}{V_{SD}-\gamma V_{ov}}}$$

[M. Castriotta, Solid State Electronics 189 (2022)]

Characterization of the FG comparator at 4.2 K

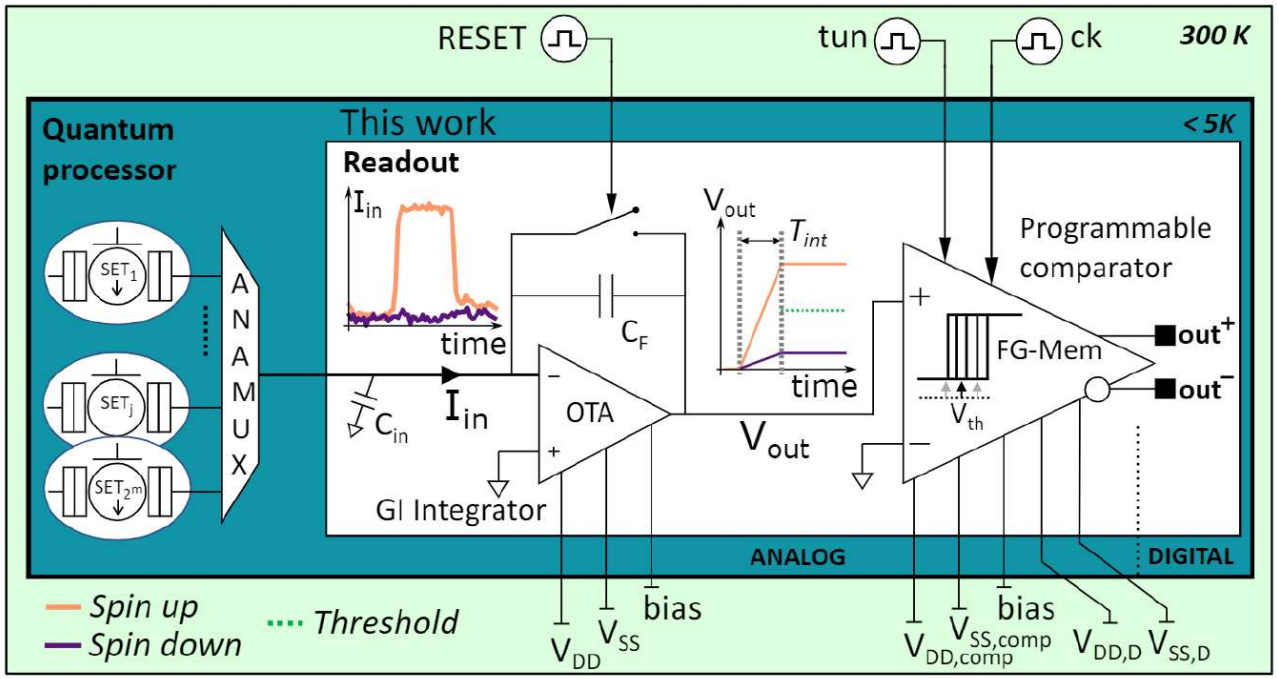


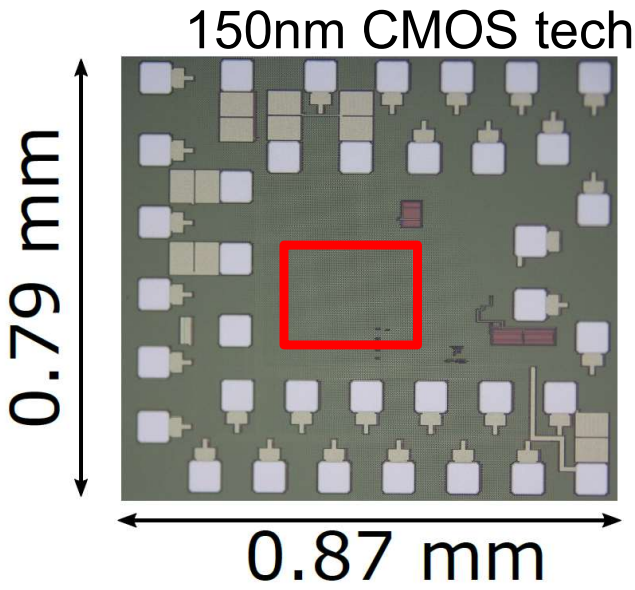
Programming accuracy: **300µV**
Sigma: **140 µV**
Calibration time**: 225 ms**
Fall/rise time**: 2 ns**



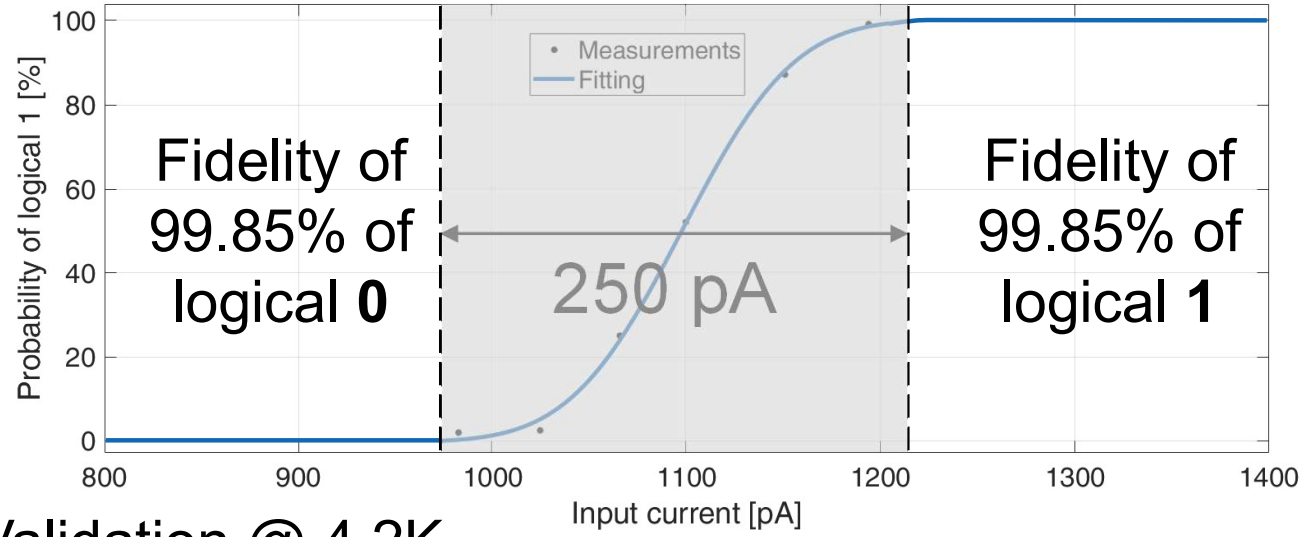
- Self-programmable threshold voltage
- Internal permanent FG memory
- "Zero" power dissipated by the memory
- Easy implementation of a TDM architecture

Characterization of the readout at 4.2 K





No off-chip components!



Validation @ 4.2K

Threshold current: **1.1 nA**
6 Sigma: **250 pA**
Readout time**: 500 ns**
Power consumption: **1.2 mW**
Active area: **0.04 mm²** (8 FGs)

[M. CASTRIOTTA et al., IEEE *Solid-state circuits letters* (2023)]

Summary

- Cryogenic CMOS circuits are feasible
  - Disadvantages:
    - higher threshold voltage
    - worse mismatch
    - poor simulation models
  - Advantages:
    - higher mobility
    - less thermal noise
    - less stray capacitances (faster devices)
- Transimpedance amplifiers (BW=30kHz, noise= 2.3pA$_{RMS}$)
- RF and baseband spin qubit readout
- … and also complex system-on-chip: see prototype of quantum controller by Intel (X. Xue et al., Nature, 2021)

Thank you for you attention!